

# Model 474DM

**40 MHz Advanced Digital Bit Sync Mezzanine**

**Tunable from 8Hz to 40 MHz, ALL PCM codes**

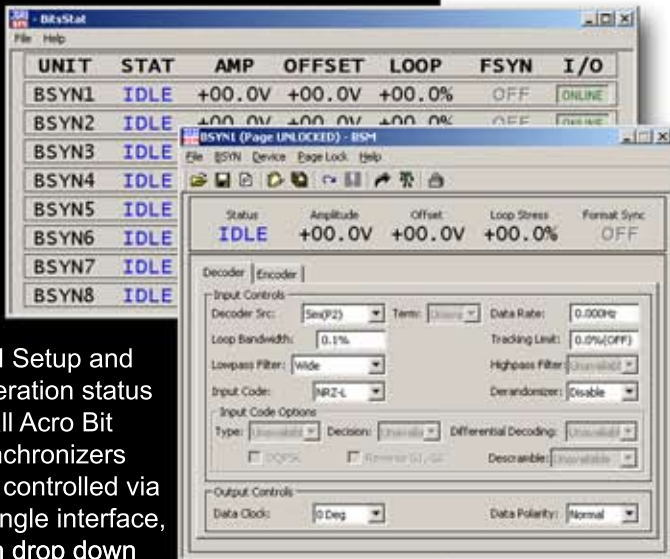
**Supports all IRIG Codes, standard and randomized**

**A second, independent encoder with TTL & Bipolar outputs**

**Viterbi, BERT, Frame Verify / QPSK options**

**Fast sync acquisition, as few as 32 bit transitions**

**Best in class noise performance**



GUI Setup and Operation status of all Acro Bit Synchronizers are controlled via a single interface, with drop down menus for individual cards. The software automatically recognizes all available bit synchronizers, as well as their features. Setup configurations can be stored and retrieved for all previous missions as a group or individually.

The 474DM Advanced Digital PCM Bit Sync is a state-of-the-art, compact "mezzanine" design created to provide range quality bit sync capabilities to Acroamatics 1602P & 1626P "single card TM processing solution" series, and expansion capability to the new Model 1611P Digital Bit Sync (dual bit syncs per PCI slot) products. 474DM is based on our new Model 1611P, and as such uses the latest techniques in FIR filtering, digital phase-locked loop, NCO clock reconstruction, and digital amplitude and offset control. Incorporating a leading-edge FPGA, the modern design delivers a greatly reduced parts count, improved reliability, and expanded capabilities. These include options normally found only in box level and full-size PCI designs - offering options such as Frame Sync Verify, Bit Error Rate Test, and Viterbi Convolutional encode/decode. The Model 474DM is a "drop-in" replacement for the 472M bit sync mezzanine, delivering superior performance and functionality.

**Full featured BERT with "live" data BER Mode**

## ACROAMATICS

## TELEMETRY SYSTEMS

# Model 474DM 40 MHz Digital Bit Synchronizer Mezzanine

## SIGNAL INPUTS

Source	Program select, 1 of 2 inputs
Isolation	Greater than 60dB at 20MHz
Impedance	Program selectable: Hi-Z/Lo-Z. Single Ended: 4k $\Omega$ /75 $\Omega$
Signal Level	0.2 to 20V p-p
DC Offset	20V max Single-ended, Hi-Z
Baseline Variation	Tracks sinusoidal offsets to 100% p-p signal amplitude at 0.1% bit rate
PCM Codes	Program selectable: NRZ-L/M/S, Bi $\phi$ -L/M/S, DBi $\phi$ -M/S, DM-M/S, MDM-M/S, RZ
Derandomizer	Program selectable: RNRZ 9/11/15/17/23, forward/reverse

## SYNCHRONIZATION

Bit Rate Range	8 bps - 40 Mbps, All PCM Codes
Tuning Resolution	0.1% of bit rate
Capture Range	3 times the programmed loopwidth, typical
Tracking Range	$\pm$ 12% typical, with programmable limiter
Loop Bandwidth	0.1% to 3.2%, program selectable in 0.1% increments
Sync Threshold	0dB for NRZ-L and Bi $\phi$ -L codes
Sync Maintenance	(LW=0.1%) -2dB NRZ-L and Bi $\phi$ -L codes
Sync Acquisition	(LW=1.6%, SNR > 12dB) Typically less than 32 bit periods
Sync Retention	(LW=0.1%, SNR > 3dB) Retains sync through > 1028 consecutive dropouts
Bit Error Rate	(LW=0.1%) to within 0.25 to 0.50 dB of ideal bit error rate performance curves

## DATA/CLOCK OUTPUTS

NRZ-L Data	Jumper Select: three TTL, one RS422/TTL
Data Clock	One each: 0 $^\circ$ , 90 $^\circ$ , 180 $^\circ$ , 270 $^\circ$ ; RS422/TTL at 0 $^\circ$ & 90 $^\circ$
Data Polarity	Program selectable: normal/inverted

## PCM ENCODER

Data Source	Program selectable: Recovered Data or External data/clock
Outputs	$\pm$ 2 Volts balanced output, 50mA drive current
Randomizer	Program selectable: RNRZ 9/11/15/17/23, forward, reverse
PCM Codes	Program selectable: NRZ-L/M/S, Bi $\phi$ -L/M/S, DBi $\phi$ -M/S, DM-M/S, MDM-M/S, RZ

## EXTERNAL DATA/CLOCK INPUT

Signal Type	Jumper selectable: RS422 or TTL
Impedance	120 $\Omega$ RS422, 75 $\Omega$ TTL
Data Code	Program selectable: NRZ-L/M/S, Bi $\phi$ -L/M/S, DBi $\phi$ -M/S, DM-M/S, MDM-M/S, RZ
Data Clock	Program selectable: Normal/Inverted, 1x or 2x

## CONVOLUTION ENCODER/DECODER (Optional)

Viterbi Decoder	Rate 1/2, k=7: includes differential decoding, V.35 descrambling, and G2 invert (others available)
Symbol Formats	serial, parallel, and staggered parallel (others available)
Convolutional Encoder	Rate 1/2, k=7: includes differential encoder, V.35 scrambler, and G2 inverter (others available)
Symbol Formats	serial, parallel, and staggered parallel (others available)

## FORMAT GENERATORS/SYNCHRONIZER (Optional)

Format Generator	Programmable frame length, sync pattern and mask
Synchronizer Source	Recovered data, external data, or test generator
Synchronizer Strategy	Pattern match in "search", programmable error limits for "check" and "lock" states
Other Features	Bit slip enable, auto polarity enable, data source/ambiguity resolution

## BIT ERROR RATE TESTER (Optional)

Transmitter Pattern	PRN sequence: PN7, PN9, PN11, PN15 (forward/reverse)
Pattern Clock Source	Program selectable: Bit Rate Clock or External Clock
Blanking	Program selectable: 64, 128, 256 bits
BER Sample Period	Program selectable: 1E3 to 1E9 bit periods, or continuous accumulate
Variable Output	50mV to 5V P-P
Other Features	Automatic pattern synchronization, forced error ON/OFF

## PHYSICAL

Hosts Supported	Plugs onto Models 1611P, 1626P & 1602P (PCI) and Legacy 1601P (PCI) & 1502V (VME) cards
Cooling Requirements	30 Linear FPM
Power Requirements	+5VDC @ 1.25A, $\pm$ 12VDC @0.25A
Dimensions	6.5" (16.51cm) H x 4.0" (10.16cm) W x .625" (1.5875cm) D
Temperature	Operating 0 to +40 $^\circ$ C, non-operating -40 to +86 $^\circ$ C
Relative Humidity	Up to 90% non-condensing
Shock	Operating 6G, Non-operating 25G
Vibration	Operating 0.3G, 5 to 2000 Hz, Non-operating 0.8G, 5 to 500 Hz

Specifications subject to change without notice