DN 6000269

TECHNICAL MANUAL
MODEL 512VE-50
• SIMULATOR/RECONSTRUCTOR •

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ACROAMATICS DOCUMENT HISTORY

The following table indicates the revision level of *Technical Manual - 512VA Simulator/Reconstructor*, Acroamatics Document Number 6000269, released on June 9, 2000, and contains a record of all revisions made since that date.

DN6000269 CHANGE HISTORY			
Rev	**Date**	**Action**	**Name**
	6-9-00	Original	DJM
	10-23-00	Added 512VE-50 data	DJM

TECHNICAL MANUAL
MODEL 512V A,B,C,D,E
• SIMULATOR/RECONSTRUCTOR •

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SECTION 1
INTRODUCTION

The various versions of the Model 512V Simulator/Reconstructor card supply a group of auxiliary functions for the Acroamatics VME Telemetry Data Processor (TDP) system. These include data stream reconstruction from data records stored in the VME Host Computer, programmable PCM frame construction for data from the system data streams, time base generation, serial data output in several formats, and DAC Bus interfacing. The card operates under control of the VME Host computer which uses the register set described in TABLE 2-1 to manage all card functions. A DMA channel that features semi-automatic buffer address chaining controls the transfer of data from memory to the TDP system's output devices located on the 512V card. Data from the DMA may be processed by the Reconstructor, the Serializer, or both. Data to the Reconstructor is formatted as two 16-bit words; the first being the ID tag portion which contains the A-bus device address that is to receive the reconstructed data, and a time interval flag that establishes a reconstructor time base. The second word is the data value. DMA messages to the PCM Serializer are also two 16-bit words. In fixed length mode, each DMA transfer provides two data messages that are serialized to form a 32-bit clock and data output that is suitable for input to the PCM Format Synchronizer. In variable length message mode, the five LSBs of the first word provide the message length and the second word contains the data for serialization, MSB justified in the 16-bit field. You can also provide messages to the Serializer in variable length format by using a PCM frame formatter memory - that constructs an output frame from user-specified data from either the distribution input bus or a specific device address on the A-bus. The Model 512V card extractor is labeled "SIMR".

1.1 Model 512V Variations

The **512VA-10 series** provide the following independent functions: a data simulator/reconstructor, a rate-programmable serializer, and five asynchronous transmit channels. Each function is offered as an option, specified by the mnemonic following the 512V model number.

The **512VB-20 series** offer all of the -10 options as well as an Inertial Navigation System (INS) data input channel.

The **512VC-30 series** offer all of the -10 and -20 features, and also provide an optional six channel synchronous transmit feature. Not all combinations are available: you cannot have both the five asynchronous channels and six synchronous channels.

The **512VD-40 series** offers a select number of available options. These include a data simulator/reconstructor, a rate-programmable serializer, five asynchronous transmit channels, and a DAC Bus interface.

The **512VE-50** is a modernized version of the 512-40 using surface mount components, and is functionally equivalent to the 512-40.

The options are described further in the following tables.

512VA-10 Options

512VA-10 SIMULATOR/RECONSTRUCTOR				
Model Number	Dash Nr	Contains Feature (Mnemonic)		
		Sim / Recon **(SR)**	Seria-alizer **(SZ)**	5 Asyn Chan **(AS)**
512VA-SR/SZ/AS	6011512-10	yes	yes	yes
512VA-SR/AS	6011512-11	yes	no	yes
512VA-SZ	6011512-12	no	yes	no

512VB-20 Options

512VB-20 SIMR				
Model Number	Dash Nr	Contains Feature (Mnemonic)		
		Sim / Recon **(SR)**	Seria-lizer **(SZ)**	INS **(IN)**
512VB-SR/SZ/IN	6011512-21	yes	yes	yes

512VC-30 Options

512VC-30 SIMR						
Model Number	Dash Nr	Contains Feature (Mnemonic)				
		Sim / Recon **(SR)**	Seria-lizer **(SZ)**	INS **(IN)**	6 Sync chans **(SY)**	5 Asyn chans **(AS)**
512VC-SR/SZ/IN/SY	6011512-31	yes	yes	yes	yes	no
512VC-SZ/SY	6011512-32	no	yes	no	yes	no
512VC-SR/SZ/AS	6011512-33	yes	yes	no	no	yes
512VC-SR/AS	6011512-34	yes	no	no	no	yes
512VC-SZ/AS	6011512-35	no	yes	no	no	yes

512VD-40 Options

512VD-40 SIMR						
Model Number	Dash Nr	Contains Feature (Mnemonic)			
		Sim / Recon **(SR)**	Seria-lizer **(SZ)**	5 Asyn chans **(AS)**	DAC Bus I/F **(DB)**
512VD-SR/SZ/AS/DB	6011512-40	yes	yes	yes	yes

512VE-50 Options

512VE-50 SIMR					
Model Number	Dash Nr	Contains Feature (Mnemonic)			
		Sim / Recon **(SR)**	Seria-lizer **(SZ)**	5 Asyn chans **(AS)**	DAC Bus I/F **(DB)**
512VE-SR/SZ/AS/DB	6011512-50	yes	yes	yes	yes

1.2 DOCUMENT CONVENTIONS

In this document register addresses and address offsets are hexadecimal numbers. Where it is necessary to refer to a hexadecimal number in the text, we use the C programming convention *0xNN* to refer to hexadecimal number *NN*. Bits in a register are numbered in decimal. The term *Device n* refers to an address destination on the TDP system A-Bus. The A-bus is the output data bus, and has eight possible destination devices. Although we do not use all eight, those destinations we do use are dedicated to specific functions in the TDP system. The term *DIT* refers to a data message in the TDP system. It stands for “Data, ID, and Time,” the three components of a TDP data message. We can label a DIT by the value of its ID tag, for example “DIT 0xFFF1,” the DIT that conveys the once per millisecond value of a time message. Frequently we use a functional label instead, for example, “the MILLISECOND DIT”.

SECTION 2
INSTALLATION

2.1 GENERAL

This section contains installation information for the Acroamatics Model 512VA Simulator/Reconstructor (SIMR). The card part number is 6011512.

2.2 UNPACKING

Using proper ESD-protection procedures, open the cardboard shipping container and remove the card from the anti-static bag. Retain the container, anti-static bag, and foam packaging material for use if you must return the card.

2.3 FACTORY RETURN

When you return a card to the factory for repair or modification, include as much information as possible describing the failure mode or the modification˜update you want.

Pack the card for shipment by wrapping it in the anti-static bag. Place the card into the shipping container, protecting it with the foam packing, and secure the container with reinforced tape. Provide the name and phone number of a technical contact we can talk to regarding the card.

Call Acroamatics at (805) 967-9909 to get an RMA number before returning any equipment to the factory, and include the number in any correspondence or shipments to Acroamatics.

2.4 INSTALLING

The SIMR card mounts in a standard VMEbus chassis. Mounting dimensions are shown in the assembly Drawing in Section 6 of this manual. Slide the card into one of your system VME chassis slots and seat the card firmly by pressing against the ears. Make the front panel cable connections appropriate to your system. Remove the board by pulling firmly on the outside of the ears.

2.5 CONNECTORS

The following pages contain tables of information on all the connections into and out of the SIMR card.

TABLE 2-1. MATING CONNECTOR LIST FOR MODEL 512VA

CONN.	FUNCTION	MATING CONNECTOR
P01	VMEbus	603-2-IEC-C096
P02	VMEbus	603-2-IEC-C096
J01	A BUS	3334-6660
J02	SERIAL CLOCK	SMB 903-285P-51S
J03	SERIAL DATA	SMB 903-285P-51S
J04	SERIAL CHANNELS	3334-6660

TABLE 2-2. CONNECTOR LIST
MODEL 512VA BACKPLANE CONNECTOR P01-ROW-A

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	4VMED00	Data Bus 00
02	4VMED01	Data Bus 01
03	4VMED02	Data Bus 02
04	4VMED03	Data Bus 03
05	4VMED04	Data Bus 04
06	4VMED05	Data Bus 05
07	4VMED06	Data Bus 06
08	4VMED07	Data Bus 07
09	GND	Ground
10	SYSCLK ($)	System Clock
11	GND	Ground
12	9VMEDS1	Data Strobe 1
13	9VMEDS0	Data Strobe 0
14	9VMEWRT	Write
15	GND	Ground
16	9VMDACK	Data Transfer Acknowledge
17	GND	Ground
18	9VMASTB	Address Strobe
19	GND	Ground
20	9VMIACK	Interrupt Acknowledge
21	9VMIAIN	Interrupt Acknowledge IN
22	9VMIAOT	Interrupt Acknowledge OUT
23	4VMAM04	Address Modifier 4
24	4VMEA07	Address Bus 07
25	4VMEA06	Address Bus 06
26	4VMEA05	Address Bus 05
27	4VMEA04	Address Bus 04
28	4VMEA03	Address Bus 03
29	4VMEA02	Address Bus 02
30	4VMEA01	Address Bus 01
31	-12 VDC ($)	-12 Volts DC
32	+5 VDC	+5 Volts DC

TABLE 2-3. CONNECTOR LIST
MODEL 512VA BACKPLANE CONNECTOR P01-ROW-B

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	9VMBSBY	Bus Busy
02	9VMBCLR	Bus Clear
03	ACFAIL ($)	AC Power Fail
04	9VMBGI0	Bus Grant 0 IN
05	9VMBGO0	Bus Grant 0 OUT
06	9VMBGI1	Bus Grant 1 IN
07	9VMBGO1	Bus Grant 1 OUT
08	9VMBGI2	Bus Grant 2 IN
09	9VMBGO2	Bus Grant 2 OUT
10	9VMBGI3	Bus Grant 3 IN
11	9VMBGO3	Bus Grant 3 OUT
12	9VMBRQ0	Bus Request 0
13	9VMBRQ1	Bus Request 1
14	9VMBRQ2	Bus Request 2
15	9VMBRQ3	Bus Request 3
16	4VMAM00	Address Modifier 0
17	4VMAM01	Address Modifier 1
18	4VMAM02	Address Modifier 2
19	4VMAM03	Address Modifier 3
20	GND	Ground
21	SERCLK ($)	Serial Clock
22	SERDAT ($)	Serial Data
23	GND	Ground
24	9VMIRQ7	Interrupt Request 7
25	9VMIRQ6	Interrupt Request 6
26	9VMIRQ5	Interrupt Request 5
27	9VMIRQ4	Interrupt Request 4
28	9VMIRQ3	Interrupt Request 3
29	9VMIRQ2	Interrupt Request 2
30	9VMIRQ1	Interrupt Request 1
31	+5 VSTDBY ($)	Stand-by +5 Volts DC
32	+5 VDC	+5 Volts DC

TABLE 2-4. CONNECTOR LIST
MODEL 512VA BACKPLANE CONNECTOR P01-ROW-C

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	4VMED08	Data Bus 08
02	4VMED09	Data Bus 09
03	4VMED10	Data Bus 10
04	4VMED11	Data Bus 11
05	4VMED12	Data Bus 12
06	4VMED13	Data Bus 13
07	4VMED14	Data Bus 14
08	4VMED15	Data Bus 15
09	GND	Ground
10	SYSFAIL ($)	System Failure
11	9VMBERR	Bus Error
12	9VMPRST	System Reset
13	9VMELWD	Long Word
14	4VMAM05	Address Modifier 5
15	4VMEA23	Address Bus 23
16	4VMEA22	Address Bus 22
17	4VMEA21	Address Bus 21
18	4VMEA20	Address Bus 20
19	4VMEA19	Address Bus 19
20	4VMEA18	Address Bus 18
21	4VMEA17	Address Bus 17
22	4VMEA16	Address Bus 16
23	4VMEA15	Address Bus 15
24	4VMEA14	Address Bus 14
25	4VMEA13	Address Bus 13
26	4VMEA12	Address Bus 12
27	4VMEA11	Address Bus 11
28	4VMEA10	Address Bus 10
29	4VMEA09	Address Bus 09
30	4VMEA08	Address Bus 08
31	+12 VDC ($)	+12 Volts DC
32	+5 VDC	+5 Volts DC

TABLE 2-5. CONNECTOR LIST
MODEL 512VA BACKPLANE CONNECTOR P02-ROW-A

PIN	SIGNAL	FUNCTION
01	4DRYOP4	ACRO PDSP4 Ready For Opcode
02	4DRYOP3	ACRO PDSP3 Ready For Opcode
03	4DRYOP2	ACRO PDSP2 Ready For Opcode
04	4DRYOP1	ACRO PDSP1 Ready For Opcode
05	9DCMRP4	ACRO PDSP4 Distribution Bus Request
06	9DCMRP3	ACRO PDSP3 Distribution Bus Request
07	9DCMRP2	ACRO PDSP2 Distribution Bus Request
08	9DCMRP1	ACRO PDSP1 Distribution Bus Request
09	9DFORCE	ACRO Data Force Flag
10	4DCMFCF	ACRO PDSP Finished With Data
11	9RFADSL	ACRO Distribution Reference Address Select
12	GND	ACRO Ground
13	9DCMWRT	ACRO Distribution Memory Write
14	4DBUS00	ACRO Distribution Data Bus 00
15	4DBUS01	ACRO Distribution Data Bus 01
16	4DBUS02	ACRO Distribution Data Bus 02
17	4DBUS03	ACRO Distribution Data Bus 03
18	4DBUS04	ACRO Distribution Data Bus 04
19	4DBUS05	ACRO Distribution Data Bus 05
20	4DBUS06	ACRO Distribution Data Bus 06
21	4DBUS07	ACRO Distribution Data Bus 07
22	GND	ACRO Ground
23	4DBUS23	ACRO Distribution Data Bus 23
24	4DBUS22	ACRO Distribution Data Bus 22
25	4DBUS21	ACRO Distribution Data Bus 21
26	4DBUS20	ACRO Distribution Data Bus 20
27	4DBUS19	ACRO Distribution Data Bus 19
28	4DBUS18	ACRO Distribution Data Bus 18
29	4DBUS17	ACRO Distribution Data Bus 17
30	4DBUS16	ACRO Distribution Data Bus 16
31	GND	ACRO Ground
32	9SRSTP1	ACRO PDSP Reset

TABLE 2-6. CONNECTOR LIST
MODEL 512VA BACKPLANE CONNECTOR P02-ROW-B

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	+5 VDC	+5 Volts DC
02	GND	Ground
03	RESERVED ($)	
04	4VMEA24	Address Bus 24
05	4VMEA25	Address Bus 25
06	4VMEA26	Address Bus 26
07	4VMEA27	Address Bus 27
08	4VMEA28	Address Bus 28
09	4VMEA29	Address Bus 29
10	4VMEA30	Address Bus 30
11	4VMEA31	Address Bus 31
12	GND	Ground
13	+5 VDC	+5 Volts DC
14	4VMED16	Data Bus 16
15	4VMED17	Data Bus 17
16	4VMED18	Data Bus 18
17	4VMED19	Data Bus 19
18	4VMED20	Data Bus 20
19	4VMED21	Data Bus 21
20	4VMED22	Data Bus 22
21	4VMED23	Data Bus 23
22	GND	Ground
23	4VMED24	Data Bus 24
24	4VMED25	Data Bus 25
25	4VMED26	Data Bus 26
26	4VMED27	Data Bus 27
27	4VMED28	Data Bus 28
28	4VMED29	Data Bus 29
29	4VMED30	Data Bus 30
30	4VMED31	Data Bus 31
31	GND	Ground
32	+5 VDC	+5 Volts DC

TABLE 2-7. CONNECTOR LIST
MODEL 512VA BACKPLANE CONNECTOR P02-ROW-C

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	9PILCK4	ACRO PDSP4 Opcode Clock
02	9PILCK3	ACRO PDSP3 Opcode Clock
03	9PILCK2	ACRO PDSP2 Opcode Clock
04	9PILCK1	ACRO PDSP1 Opcode Clock
05	9DCMAK4	ACRO PDSP4 Distribution Bus Acknowledge
06	9DCMAK3	ACRO PDSP3 Distribution Bus Acknowledge
07	9DCMAK2	ACRO PDSP2 Distribution Bus Acknowledge
08	9DCMAK1	ACRO PDSP1 Distribution Bus Acknowledge
09	9RSTFFL	ACRO Data Force Reset
10	9TSTMOD	ACRO PDSP Test Mode
11		Not Used
12	GND	ACRO Ground
13	9DSEQ02	ACRO ID-Data Output Enable
14	4DBUS08	ACRO Distribution Data Bus 08
15	4DBUS09	ACRO Distribution Data Bus 09
16	4DBUS10	ACRO Distribution Data Bus 10
17	4DBUS11	ACRO Distribution Data Bus 11
18	4DBUS12	ACRO Distribution Data Bus 12
19	4DBUS13	ACRO Distribution Data Bus 13
20	4DBUS14	ACRO Distribution Data Bus 14
21	4DBUS15	ACRO Distribution Data Bus 15
22	GND	ACRO Ground
23	4DBUS31	ACRO Distribution Data Bus 31
24	4DBUS30	ACRO Distribution Data Bus 30
25	4DBUS29	ACRO Distribution Data Bus 29
26	4DBUS28	ACRO Distribution Data Bus 28
27	4DBUS27	ACRO Distribution Data Bus 27
28	4DBUS26	ACRO Distribution Data Bus 26
29	4DBUS25	ACRO Distribution Data Bus 25
30	4DBUS24	ACRO Distribution Data Bus 24
31	GND	ACRO Ground
32	9SCLKP1	ACRO PDSP Clock

TABLE 2-8. CONNECTOR LIST
MODEL 512VA FRONT PANEL CONNECTOR J01

PIN	SIGNAL	FUNCTION
01		Not Used
02	9AWORD1	A Bus Last Word Flag
03	4SFLAG1	A Bus Last Transfer Flag
04	4APORT1	A Bus Port Select 1
05	GND	Ground
06	4APORT0	A Bus Port Select 0
07	4ADEST2	A Bus Destination Select 2
08	4ADEST1	A Bus Destination Select 1
09	4ADEST0	A Bus Destination Select 0
10	4AOUT15	A Bus 15
11	4AOUT14	A Bus 14
12	GND	Ground
13	4AOUT13	A Bus 13
14	4AOUT12	A Bus 12
15	4AOUT11	A Bus 11
16	4AOUT10	A Bus 10
17	GND	Ground
18	4AOUT09	A Bus 09
19	4AOUT08	A Bus 08
20	4AOUT07	A Bus 07
21	4AOUT06	A Bus 06
22	4AOUT05	A Bus 05
23	4AOUT04	A Bus 04
24	GND	Ground
25	4AOUT03	A Bus 03
26	4AOUT02	A Bus 02
27	4AOUT01	A Bus 01
28	4AOUT00	A Bus 00
29	GND	Ground
30	9AOACK0	A Bus Acknowledge 0
31	9AOREQ0	A Bus Request 0
32	GND	Ground
33	9AOACK1	A Bus Acknowledge 1
34	9AOREQ1	A Bus Request 1
35	GND	Ground
36	9AOACK2	A Bus Acknowledge 2
37	9AOREQ2	A Bus Request 2
38	GND	Ground
39	9AOACK3	A Bus Acknowledge 3
40	9AOREQ3	A Bus Request 3

TABLE 2-8. (continued) CONNECTOR LIST
MODEL 512VA FRONT PANEL CONNECTOR J01

NOTE: ALL ($) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
41	GND	Ground
42	9AOWAIT	A Bus Wait
43	9AOREST	A Bus Reset
44	GND ($)	Ground
45		Not Used
46		↓
47		↓
48		↓
49		↓
50		↓
51		↓
52		↓
53		↓
54		↓
55		↓
56		↓
57		↓
58		Not Used
59	GND	Ground
60	9AOSTRB	A Bus Data Strobe

TABLE 2-9. CONNECTOR LIST
MODEL 512V FRONT PANEL CONNECTOR J02

PIN	SIGNAL	FUNCTION
01	4PCMCLK	Serial Clock Out
02	GND	Ground

TABLE 2-10. CONNECTOR LIST
MODEL 512VA FRONT PANEL CONNECTOR J03

PIN	SIGNAL	FUNCTION
01	4PCMDAT	Serial Data Out
02	GND	Ground

USE THIS J04 LIST WITH 6011512-10, 11, 33, 34, 35 CARDS (No channels or 5 aysnchronous channels)

TABLE 2-11. CONNECTOR LIST
MODEL 512V FRONT PANEL CONNECTOR J04

FOR MODELS 512VA-10, 11 or 512VC-33, 34, 35

PIN	SIGNAL	FUNCTION
01		Not used
↓	↓	↓
37		Not used
38	4DATA01	485 Data, Serial channel +01
39	9DATA01	485 Data, Serial channel -01
40	RGND001	Not used
41	RGND001	Not used
42	4DATA02	485 Data, Serial channel +02
43	9DATA02	485 Data, Serial channel -02
44	RGND002	Not used
45	RGND002	Not used
46	4DATA03	485 Data, Serial channel +03
47	9DATA03	485 Data, Serial channel -03
48	RGND003	485 Ground
49	RGND003	485 Ground
50	4DATA04	485 Data, Serial channel +04
51	9DATA04	485 Data, Serial channel -04
52	RGND004	485 Ground
53	RGND004	485 Ground
54	4DATA05	485 Data, Serial channel +05
55	9DATA05	485 Data, Serial channel -05
56	4CLOCK5	485 Clock, Serial channel +05
57	9CLOCK5	485 Clock, Serial channel -05
58	4SYNCH5	485 Synch, Serial channel +05
59	9SYNCH5	485 Synch, Serial channel -05
60	RGND005	485 Ground

USE THIS J04 LIST WITH 6011512-21 CARD (INS)

TABLE 2-12. CONNECTOR LIST
MODEL 512V FRONT PANEL CONNECTOR J04

FOR VERSION 512VB-21

PIN	SIGNAL	FUNCTION
01		NC
↓	↓	↓
45		NC
46	4INSDAT	INS Data Input +
47	9INSDAT	INS Data Input -
48	GND	Signal Ground
49	GND	Signal Ground
50	4INSCLK	INS Clock Input +
51	9INSCLK	INS Clock Input -
52	GND	Signal Ground
53	4INSSYC	INS Word Sync +
54	9INSSYC	INS Word Sync -
55		NC
56		NC
57		NC
58		NC
59		NC
60		NC

USE THIS J04 LIST WITH 6011512-31, 32 CARDS (INS and˜or 6 synchronous channels)

TABLE 2-13. CONNECTOR LIST
MODEL 512VC FRONT PANEL CONNECTOR J04

FOR VERSION 512VC-31, 32

PIN	SIGNAL	FUNCTION
01	9DCDETA	CH A Carrier Detected
02	9RCCLKA	CH A Receive Clock
03	9RCDATA	CH A Receive Data
04	9RTSNDA	CH A Request to send
05	9XTDATA	CH A Transmit Data
06	9DTRDYA	CH A Terminal Ready
07	Ground	
08	9DCDETB	CH B Carrier Detected
09	9RCCLKB	CH B Receive Clock
10	9RCDATB	CH B Receive Data
11	9RTSNDB	CH B Request to send
12	9XTDATB	CH B Transmit Data
13	9DTRDYB	CH B Terminal Ready
14	Ground	
15	9DCDETC	CH C Carrier Detected
16	9RCCLKC	CH C Receive Clock
17	9RCDATC	CH C Receive Data
18	9RTSNDC	CH C Request to send
19	9XTDATC	CH C Transmit Data
20	9DTRDYC	CH C Terminal Ready
21	Ground	
22	9DCDETD	CH D Carrier Detected
23	9RCCLKD	CH D Receive Clock
24	9RCDATD	CH D Receive Data
25	9RTSNDD	CH D Request to send
26	9XTDATD	CH D Transmit Data
27	9DTRDYD	CH D Terminal Ready
28	Ground	
29	9DCDETE	CH E Carrier Detected
30	9RCCLKE	CH E Receive Clock
31	9RCDATE	CH E Receive Data
32	9RTSNDE	CH E Request to send
33	9XTDATE	CH E Transmit Data
34	9DTRDYE	CH E Terminal Ready
35	Ground	
36	9DCDETF	CH F Carrier Detected

TABLE 2-13. (continued) CONNECTOR LIST
MODEL 512VC FRONT PANEL CONNECTOR J04

FOR VERSION 6011512-31 & -32

PIN	SIGNAL	FUNCTION
37	9RCCLKF	CH F Receive Clock
38	9RCDATF	CH F Receive Data
39	9RTSNDF	CH F Request to send
40	9XTDATF	CH F Transmit Data
41	9DTRDYF	CH F Terminal Ready
42	Ground	
43		NC
44		NC
45		NC
46	4INSDAT	INS Data Input +
47	9INSDAT	INS Data Input -
48	GND	Signal Ground
49	GND	Signal Ground
50	4INSCLK	INS Clock Input +
51	9INSCLK	INS Clock Input -
52	GND	Signal Ground
53	4INSSYC	INS Word Sync +
54	9INSSYC	INS Word Sync -
55		NC
56		NC
57		NC
58		NC
59		NC
60		NC

USE THIS J04 LIST WITH 6011512-40 & -50 CARDS ONLY

TABLE 2-13. CONNECTOR LIST
MODEL 512VD/VE FRONT PANEL CONNECTOR J04

FOR VERSIONS 512VD-40 & 512VE-50 ONLY

PIN	SIGNAL	FUNCTION
01	9DAAB13	DAC Address Bit 13
02	9DACACK	DAC Bus Wait
03	GND	Ground
04	9DAAB0	DAC Address Bit 0
05	9DAAB15	DAC Address Bit 15
06	9DAAB14	DAC Address Bit 14
07	9DAAB12	DAC Address Bit 12
08	9DAAB11	DAC Address Bit 11
09	9DAAB10	DAC Address Bit 10
10	9DAAB9	DAC Address Bit 9
11	9DAAB8	DAC Address Bit 8
12	9DAAB7	DAC Address Bit 7
13	9DAAB6	DAC Address Bit 6
14	9DAAB5	DAC Address Bit 5
15	9DAAB4	DAC Address Bit 4
16	9DAAB3	DAC Address Bit 3
17	9DAAB2	DAC Address Bit 2
18	9DAAB1	DAC Address Bit 1
19	9DATSTB	DAC Data Strobe
20	GND	Ground
21	9DADB15	DAC Data Bit 15
22	9DADB14	DAC Data Bit 14
23	9DADB13	DAC Data Bit 13
24	9DADB12	DAC Data Bit 12
25	9DADB11	DAC Data Bit 11
26	9DADB10	DAC Data Bit 10
27	9DADB9	DAC Data Bit 9
28	9DADB8	DAC Data Bit 8
29	9DADB7	DAC Data Bit 7
30	9DADB6	DAC Data Bit 6
31	9DADB5	DAC Data Bit 5
32	9DADB4	DAC Data Bit 4
33	9DADB3	DAC Data Bit 3
34	9DADB2	DAC Data Bit 2
35	9DADB1	DAC Data Bit 1
36	9DADB0	DAC Data Bit 0
37	9DACAEB	DAC Address Cycle

See Section 3.12, DAC Bus I/F, for details.

continued next page...

TABLE 2-13. CONNECTOR LIST (continued)
MODEL 512VD/VE FRONT PANEL CONNECTOR J04

FOR VERSIONS 512VD-40 & 512VE-50 ONLY

PIN	SIGNAL	FUNCTION
38	4DATA01	485 Data, Serial channel +01
39	9DATA01	485 Data, Serial channel -01
40	RGND001	Not used
41	RGND001	Not used
42	4DATA02	485 Data, Serial channel +02
43	9DATA02	485 Data, Serial channel -02
44	RGND002	Not used
45	RGND002	Not used
46	4DATA03	485 Data, Serial channel +03
47	9DATA03	485 Data, Serial channel -03
48	RGND003	485 Ground
49	RGND003	485 Ground
50	4DATA04	485 Data, Serial channel +04
51	9DATA04	485 Data, Serial channel -04
52	RGND004	485 Ground
53	RGND004	485 Ground
54	4DATA05	485 Data, Serial channel +05
55	9DATA05	485 Data, Serial channel -05
56	4CLOCK5	485 Clock, Serial channel +05
57	9CLOCK5	485 Clock, Serial channel -05
58	4SYNCH5	485 Synch, Serial channel +05
59	9SYNCH5	485 Synch, Serial channel -05
60	RGND005	485 Ground

See Section 3.8, Asynchronous Data, for details

SECTION 3
OPERATION

3.1 INTERFACE REGISTER SET

This section describes the arrangement and functions of the register set on the 512VA card. TABLE 3-1 lists the registers in address order, showing A16 utility space allocation. The address shown is the offset address (in hexadecimal) from the card base address set by switches on the card.

A16 Utility Registers		
Addr	**Function**	**Mode**
00	Signature	Read only
02	CVT Memory A32 Base Address	Read/Write
04	DMA Command/Status	Read/Write
06	Interrupt Vector	Read/Write
08	DMA Primary Address (A31-A16)	Read/Write
0A	DMA Primary Address (A15-A2)	Read/Write
0C	DMA Backup Address (A31-A16)	Write Only
0E	DMA Backup Address (A15-A2)	Write Only
10	DMA Primary Word Count	Read/Write
12	DMA Backup Word Count	Write Only
14	Time Base Generator Control	Read/Write
16	Time-of-Year Days and Hours	Read/Write
18	Time-of-Year Minutes and Seconds	Read/Write
1A	Time-of-Year Tenths of Milliseconds	Read/Write
1C	Reconstructor Control	Read/Write
1E	Reconstructor Status	Read Only
20	Frame Buffer Control	Read/Write
22	Frame Buffer Mask Register	Read/Write
24	Frame Interval Register	Read/Write
26	Spare	Read/Write
28	Serializer Rate	Read/Write
2A	Serializer Control	Read/Write
2C	Bits Per Frame	Write Only
2E	0.5% Frame Window	Write Only
30	Asynchronous Channels 1 & 2 Control	Read/Write
32	Asynchronous Channels 3 & 4 Control	Read/Write
34	Asynchronous Channel Select	Write Only
36	INS Control	Read/Write
38	Transmitter Control	Read/Write
3A	Channel Selection 1-4	Read/Write
3C	Channel Selection 5-8	Read/Write
3E	Bits Per Frame	Read/Write

TABLE 3-1. Simulator/Reconstructor Interface A16 Registers

The registers contain 512VA *command* and *status* information. Register locations are memory-mapped in the A16 Utility Address Space on a switch-selectable 64-byte boundary. You access the registers through nonprivileged or supervisory A16/D16 memory instructions.

3.1.1 Signature Register (Address 00)

The Signature Register identifies the installed 512VA card for system configuration purposes. Reading this register returns a value of 0x512, that is the bit pattern *XXXX010100010010*. The four *XXXX* bits identify the installed options. You should mask these bits during any card identification function.

Signature Register		
Addr	**Description**	**Mode**
0	X512	Read

TABLE 3-2. Signature Register

Signature Register Option Bits	
Bit	**Description**
15	Not Used
14	Synchronous Comm Installed
13	Serializer Installed
12	Reconstructor Installed

TABLE 3-3. Option Bits in Signature Register

3.2 SIMR VME DMA SYSTEM

The input DMA system on the 512VA card is a one way transfer of data from VME memory to the reconstructor and PCM serializer FIFOs; it does not transfer data into VME memory.

A 32-bit counter register called the *Primary Address Register* always contains the address of the next location to be accessed in VME memory. Two 16-bit transfers to the Primary Address Register (at address offsets 08 and 0A) load the starting A32 address for a block transfer. The Primary Address Register indicates it is loaded (DMA Status Register bit 8 reads as 1) upon loading the least significant 16 bits into address 0A.

A 16-bit *Primary Word Count* register holds the number of 32-bit words awaiting transfer from VME memory. (load this register with zero for a transfer count of 65536). When the Primary Address Register has loaded status and the DMA Interface is enabled, the DMA transfers initiate. You should load the Primary Word Count register previous to this. The 32-bit *Backup Address* register (formed by addresses 0C and 0E) holds the starting A32 address for the *next* block transfer that will occur after the *primary* transfer is complete. The 16-bit *Backup Count* register (address 12) contains the transfer length of that next block transfer.

the Primary Address register auto-increments with each DMA transfer. The Primary Word Counter auto-decrements until it reaches zero, signifying completion of the DMA transfer. If the Backup Address register is loaded, it's contents are transferred to the Primary Address Register while, in a similar fashion, the Backup Count register contents are transferred to the Primary Count Register and the DMA transfer continues. When the Backup Address register is empty the DMA transfer stops. In either case, an interrupt occurs if the DMA Terminal

Count Interrupt is enabled.

The Backup Address register becomes loaded (DMA Status Register bit 9 reads as 1) when you load the least significant half (address 0E). A reasonable loading order is Backup Count, Backup Address MSH, and then Backup Address LSH. If the Primary Address is not loaded, the DMA is idle and the Backup Registers transfer immediately to the Primary Registers. If the Primary Address is loaded, the Backup Address retains *loaded* status until the DMA block transfer completes and the Backup Registers transfer to the Primary Registers. You then reload the Backup Registers. Thus you can consider the Primary and Backup registers a two location queue. You never have to load the Primary registers directly when you are performing double-buffered data transfers. For single buffered operation it is more convenient to use the Primary registers.

3.2.1 DMA Command/Status Register (Address 04)

The DMA Command/Status Register (CSR) provides control for the DMA interface, along with *enable* and *status* signals for the interrupt structure. TABLE 3-4 lists the *command* and *status* bits of the register. To the extent possible, the DMA control is identical to that of the 504VA DIST Card.

DMA Command/Status Register		
Bit	**Function**	**Mode**
15-12	Not used	
11	DMA Interface Enable	Read/Write
10	DMA Interface Reset	Write Only
9	DMA Backup Address Loaded Status	Read Only
8	DMA Primary Address Loaded Status	Read
8	Enables writing of Bit 11	Write
7	Enables writing Bits 0, 1 & 2	Write only
6	Enables clearing of Bits 3, 4 & 5	Write only
5	Not Used	
4	Reconstructor Tick Interrupt Status	Read Only
3	DMA Terminal Count Interrupt Status	Read Only
2	Not Used	
1	Reconstructor Tick Interrupt Enable	Read/Write
0	DMA Terminal Count Interrupt Enable	Read/Write

TABLE 3-4. DMA Command/Status Register

The following bit descriptions describe the condition that results when you set the specified command bit to **1**. For a status bit, the state described exists when you read the specified bit as **1**. Some bits have both a command and a status function.

Bits 15 through 12 - Not used

Bit 11 - Command: enables the DMA to the Reconstructor and/or the PCM Serializer.

Bit 10 - Command: clears the DMA Primary and Backup Address Loaded status.

Bit 9 - Status: the DMA Backup Address is loaded.

Bit 8 - Status: the DMA Primary Address is loaded.
Command: enables you to write to Command bit 11.

Bit 7 - Command: enables you to write bits 2, 1, & 0 of the register.

Bit 6 - Command: clears the current interrupt status, bits 5-3.

Bit 5 - Not used.

Bits 4 & 3 - Status: records the source or sources of an interrupt. The bits remain set until cleared by writing **1** to bit 6. If another interrupt causing-event occurs before the Interrupt Status bits are cleared, the interrupt controller queues the second interrupt and its sources until the current interrupt status is cleared. An interrupt from a given source occurs only if the corresponding Interrupt Enable bit is set to **1**. If the Interrupt Enable bit is not **1**, the corresponding status bit cannot be set.

Bit 4 - Status: the Reconstructor Tick Interval Counter reached zero.

Bit 3 - Status: the DMA Primary Word Count reached zero.

Bits 1 and 0 - are the enables for the two possible interrupt sources. Bit 7 of the CSR must be set to **1** when programming these bits.

Bit 2 - Not used.

Bit 1 - Command: allows an interrupt when the Reconstructor Tick Interval Counter reaches zero.

Bit 0 - Command: allows an interrupt when DMA Primary Word Count reaches zero.

3.2.2 Interrupt Vector Register (Address 06)

The Interrupt Vector Register holds a 16-bit address that addresses the memory cell containing the address of the common interrupt service routine that services all three possible interrupts from the 512VA card.

3.3 TIME BASE GENERATOR FEATURE

The Model 512VA has a Time Base Generator that delivers time messages to the input data stream (Feedback Port) or to the output data stream (A-bus) at programmable intervals. In the TDP system you use messages called **DITs** to supply a reference against which you can relate data samples flowing through the system to real-time. You choose either or both of two A-bus addresses to which the DIT is sent. The generator also supplies interval timing to an output data stream (A-bus Device 0) or injects it into the TDP input section (via the Feedback Port) where the Programmable Data Stream Processor uses the interval timing for annotation purposes. With this feature, you can annotate data with time even if you have no 503V TIME (Time Code Generator/Translator) card in the system.

You set up the Generator to produce three message types which produce 4 DITs, each with a reserved ID tag.

1. Arbitrary programmable interval messages. DIT type 4 is called an INTERVAL DIT. (We abbreviate that to “INT DIT”.) We intend it to allow you to cause an event that happens at an interval that you choose. The interval is programmable from one microsecond to 1024 milliseconds. The DIT has a reserved ID tag of 0xFFF0 that the VME TDP system does not

presently use.

2. Time-of-year messages. When you enable time-of-year messages, the generator outputs both a once per millisecond DIT (type 2, with ID tag 0xFFF2), and a once per second DIT (type 1, with ID tag 0xFFF3). These correspond to DITs generated by the 503V TIME card, although the ID tags are different from those the 503V generates. We intend this feature to allow you to use this card instead of the TGT if you do not require IRIG Time Code translation, only a real-time time base.

3. Ten times per millisecond messages. DIT (type 3) supplies a .1 millisecond time base using ID tag 0xFFF1.

3.3.1 Time Base Generator Control Register (Address 14)

The Time Base Generator Control Register supplies program control of the Generator. Bits 0-9 of this register are a 10-bit binary interval count value. This count reloads the interval counter which counts either a once per millisecond or once per microsecond clock. When the counter reaches zero, the Time Base Generator generates an INT DIT message and sends it to A-bus Device 4. Device 4 connects to the VME TDP system's input data bus by way of an input register called the Feedback port.

When bit 10 is a **0**, the counter counts microseconds. When it is a **1**, the counter counts milliseconds.

Time messages have four different formats called Time DIT types 1, 2, 3, and 4. These are shown in TABLES 3-7 through 3-10. Bits 11 through 15 select these formats as shown in TABLE 3-5 below.

Time Base Generator Control Register	
Bit	**Function**
15	Output the INT DIT to Device 4, the Feedback port
14	Output the 100μs DIT to Device 0, the Host Interface
13	Output the 1ms DIT to Device 0, the Host Interface
12	Output the 100μs DIT to Device 4, the Feedback port
11	Output the 1ms DIT to Device 4, the Feedback port
10	Interval counter rate (count ms)
9 ↓ 0	INT DIT Interval Count Field (in binary)

TABLE 3-5. Time Base Generator Control Register

Bit 15 - set bit 15 to **1** when you want the INT DIT. Store a non-zero value in the interval count field to generate a Type 4 DIT at the programmable interval to Device 4 with ID tag 0xFFF0.

Bit 14 - output a Type 3 DIT at 100 microsecond intervals to Device 0 with ID tag 0xFFF1.

Bit 13 - output a Type 2 DIT at 1 millisecond intervals to Device 0 with ID tags

0xFFF2, and a Type 1 DIT with ID tag 0xFFF3 at one second intervals.

Bit 12 - output a Type 3 DIT at 100 microsecond intervals to Device 4 with ID tag 0xFFF1.

Bit 11 - output a Type 2 DIT at 1 millisecond intervals to Device 4 with ID tag 0xFFF2, and a Type 1 DIT with ID tag 0xFFF3 at 1 second intervals.

Bit 10 - the interval counter counts milliseconds when this bit is set to **1**, and microseconds when set to **0**.

Bits 9 through 0 - contain a binary count which controls the number of microseconds or milliseconds in an interval.

When you enable the 100 microsecond DIT, the Generator outputs a DIT with the ID tag 0xFFF1 at 100 μsecond intervals. When you enable the 1 millisecond DIT, the Generator outputs a DIT with the ID tag 0xFFF2 every millisecond and preceding millisecond 0 a DIT with the ID tag 0xFFF3. If you enable the 100 microsecond DIT, the 0 microsecond message follows the millisecond message. If you want the TDP system to annotate data to .1 millisecond resolution, bits 11 and 12 must be set to **1**.

3.3.2 Time-Of-Year Data Registers (Address 16, 18, 1A)

The three registers at addresses 16, 18, 1A access a time of year counter that computes the current time-of-year in BCD. These three registers supply the data that appears in the time DITs. The Host Computer loads these registers to preset the time-of-year. Register 16 contains days and hours; register 18, minutes and seconds; and register 1A, tenths of milliseconds.

The BCD time formats which you preset into registers 16 through 1A are shown in TABLE 3-6 below.

Time Words				
Data Bits				**Description**
15 - 12	11 - 8	7 - 4	3 - 0	
Register 16				
x x x x	x x x x	x x x x	x x x x	MAJOR TIME: DAYs, HOURs
x x x x				Tens of Days (BCD)
	x x x x			Units Days (BCD)
		x x		Tens of Hours (0-2)
		x x	x x	Units Hours (BCD)
			x x	Hundreds of Days (0-3)
Register 18				
x x x x	x x x x	x x x x	x x x x	MAJOR TIME: MINs, SECs
x x x x				Tens of Minutes (0-5)
	x x x x			Units Minutes (BCD)
		x x x x		Tens of Seconds (0-5)
			x x x x	Units Seconds (BCD)
Register 1A				
x x x x	x x x x	x x x x	x x x x	MILLISECONDS WORD
x x x x				Milliseconds Hundreds (BCD)
	x x x x			Milliseconds Tens (BCD)
		x x x x		Milliseconds Units (BCD)
			x x x x	Milliseconds Tenths (BCD)

TABLE 3-6. Time-Of-Year Register Formats

Tables 3-7 through 3-10 on the following page show the message formats for the four time message DITs. Although we refer to the data word that contains the millisecond annotation as “Millisecond,” it actually contains a .1 millisecond field so it is really BCD tenths of milliseconds. When the DITs occur simultaneously on the millisecond and on the second, the Generator outputs as many of the DITs as are enabled. For example, if you enable .1 millisecond and millisecond, on the one second boundary DITs 0xFFF3, 0xFFF2, and 0xFFF1 are all output. This is done so that the Programmable Data Stream Processor (PDSP) software that is interested in only one of the time bases does not have to process any of the others.

Word	Output each second
1	0
2	ID Tag 0xFFF3
3	Register 16 (Days, Hrs)
4	Register 18 (Min, Sec)

TABLE 3-7. One Second DIT (Type 1)

Word	Output each millisecond
1	0
2	ID 0xFFF2
3	Register 1A (Millisecond)
4	Register 18 (Min, Sec)

TABLE 3-8. 1 MS DIT (Type 2)

Word	Output each 100 microseconds
1	0
2	ID 0xFFF1
3	Register 1A (Millisecond)
4	Register 18 (Min, Sec)

TABLE 3-9. 100 μS DIT (Type 3)

Word	Output at programmable interval
1	0
2	ID 0xFFF0
3	Register 1A (Millisecond)
4	Register 18 (Min, Sec)

TABLE 3-10. Interval DIT (Type 4)

3.4 RECONSTRUCTOR FEATURE

The Reconstructor section of the 512VA card accepts data via the DMA into a FIFO, then outputs the FIFO data to the A-bus. The three MSB bits of the Reconstruction Control Register (Address 1C) select which of the *reconstruction modes* will determine the A-bus output devices that you can address, as well as how you use specific portions of the ID tag. If all three bits are set to **0** you can access output device addresses 0, 4, 5, or 7. You must provide these various destinations when you construct the data stream ID tags according to a convention encoding the target destinations into the ID tags. The Reconstructor uses bits 14 and 15 of the ID tag field of the DIT to provide this routing information. These two bits select the output device as follows.

BIT 15	BIT 14	DEVICE
1	1	DAC Inputs (Device 7)
1	0	Feedback Port (Device 4)
0	1	Serializer (Device 5)
0	0	Host Interface (Device 0)

This scheme allows your data stream to contain a mix of (1) fully decommutated, ID tagged data with up to 8192 unique ID tags, and (2) partially decommutated data you want to route to the special devices on the A-bus during reconstruction.

During *record* operations, the reconstructor generates the time interval DIT (at your specified interval) and merges the DIT (with bit 13 set to **1**) into the output stream while the reconstructor is acquiring the data you want it to recreate. The reserved ID tag 0x1FFF0 is assigned to the interval DIT.

During *playback*, bit 13 of the ID tag is the time interval “tick” flag, which the reconstructor uses to synchronize the flow of data to real-time. The Reconstructor synchronizes its DMA-supplied data stream by testing bit 13 of the ID tag field of the DIT. When bit 13 is set to **1**, the reconstructor waits (for your program-selected time interval) before proceeding with the reconstruction of data from the input FIFO. The DIT carrying the tick bit is discarded by the Reconstructor. The Reconstructor uses its interval counter to synchronize the extraction of data from the FIFO. When the Reconstructor first encounters a tick in the FIFO it presets the interval counter to the user-programmed value in the Reconstructor Control Register. The reconstructor processes the FIFO data up to the next tick. There it waits for the Interval Counter to count to zero, then presets it again and continues. If the counter reaches zero before the next tick arrives, the Reconstructor has fallen behind the data stream. This is an error condition, and the Reconstructor sets an error status bit in the control register. There is also a mode in which the Reconstructor processes successive DITs at a fixed programmable interval.

If any one of the three MSBs of the Reconstruction Control register is set to **1** Device 4 becomes the only accessible A-bus address. This allows the stream of decommutated ID tagged data with up to 64k unique ID tags. The actual size of the ID field on the reconstructed data is determined by the setting of the three MSBs of the Reconstruct Control register as follows: Bit 15 set to **1** selects 13 bit ID tags; bit 14 set to **1** selects 12 bit ID tags; and Bit 13 set to **1** selects 16 bit ID tags.

Bit 13 of the ID tag can be used as an ID tag, in which case it cannot be used as the *time interval* flag as previously described. In this mode the time interval DIT is indicated by the reserved ID tag 0xFFF0, the reserved ID tag for the time interval DIT.

3.4.1 Reconstructor Control Register (Address 1C)

This register contains a 10-bit binary interval count and a microsecond/millisecond flag (bit 10). When the flag is set to **1** the 10-bit count is milliseconds per tick; when set to **0** the count is microseconds per tick. This register can be set to match the time interval of the ticks in the data stream that are DMA transferred to the hardware Reconstructor.

Reconstructor Control Register	
Bit	**Function**
15	Select Device 4 - 13 bit ID
14	Select Device 4 - 12 bit ID
13	Select Device 4 - 16 bit ID
12	Input Tick Enable
11	Reconstructor Enable
10	Interval counter rate (count milliseconds)
9 ↓ 0	Counter Interval In Binary

TABLE 3-11. Reconstructor Control Register

Bits 15 through 13 - These bits are unique *set bits* in that only one bit can be set to **1** at a time. If any one of these bits is set to **1**, A-bus Device 4 is the only output device that can be addressed. The two MSBs of the ID tag select the output device when all three bits are set to **0**.

Bit 15 - When this bit is set to **1**, reconstructed data is sent to Device 4 and the *three* MSB ID bits are masked to 0 (Bits 47-45 of Device 4 word format).

Bit 14 - When set to **1**, routes reconstructed data to Device 4 and the *four* MSB ID bits are masked to 0 (Bits 47-44 of Device 4 word format).

Bit 13 - When set to **1**, routes reconstructed data to Device 4 and passes the entire 16 bit ID tag.

Bit 12 - Enables the Reconstructor to use the tick bit from the input FIFO to reconstruct a time base when set to **1**. When this bit is set to **0**, the Reconstructor reads one DIT from the input FIFO and delivers it to the A-bus each time the counter reaches zero.

Bit 11 - Set to **1** to enable data from the DMA to go into the input FIFO and start the reconstruction of the data.

Bit 10 - the interval counter counts milliseconds when this bit is set to **1**, and microseconds when set to **0**.

Bits 9 through 0 - contain a binary count which controls the number of microseconds or milliseconds in the counter interval.

3.4.2 Reconstructor Status Register(Address 1E)

Reconstructor Status Register	
Bit	**Function**
15	Reconstructor Overflow
14	Input FIFO Not Empty
13	Output FIFO Not Empty
12-0	Not Used

TABLE 3-12. Reconstructor Status Register

Bit 15 - At some time the input stream contained more data samples than could be processed in the selected time interval. This bit is cleared when read.

Bit 14 - The Reconstructor Input FIFO is Not Empty.

Bit 13 - The Reconstructor Output FIFO is Not Empty.

3.5 DATA SERIALIZER FEATURE

The data Serializer accepts data from either the frame buffer memory or the DMA channel and outputs that data as a semi-synchronous serial data stream. It generates clock and data at a programmable rate from .5 bits per second to 32 megabits per second. The serializer outputs 1 to 16 bits (plus parity, when enabled) as a msb- or lsb-ordered serial word. The parallel input word can be right-justified (lsb in bit 0) or left-justified (msb in bit 15) for word lengths less than 16 bits.

3.5.1 Serializer Modes

You can use the Serializer in several software-selectable ways.

1. You can drive the Serializer with 32-bit raw data coming from Host memory by way of the DMA channel. In this mode the serializer forms a low cost PCM data simulator or disk storage Reconstruct system.
2. You can use the DMA with formatted messages. The message contains a 16-bit data field and a 15 bit control word.
3. You can drive the Serializer with *asynchronous input* data from the TDP by outputting user-defined frames of PCM data, created from incoming data that has been stored in the current value memory portion of the frame buffer memory. The synchronous time-division-multiplexed PCM frame contains the last value of the input data selected for that time slot. The output frame rate is determined by the serializer bit rate.
4. You can use the Serializer in *synchronous input* mode. The frame buffer memory reformats and outputs the PCM frame in synchronous mode. This allows you to output user defined input words in an arbitrary sequence. The frame buffering allows the serial output rate to be adjusted to correct for rate discrepancies. The programmable output frame is terminated by a *frame end* signal that the Serializer servos the bit rate to - thereby holding a constant interval between the frame signals transmitted with the data. In other words, the output frame rate is determined by the

input frame rate.

The input message formats described above are shown in TABLES 3-13 & 3-14 below.

32 BIT DMA WORD (MODE 1)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
First Serial Word															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Second Serial Word															

TABLE 3-13. Input Message Format for Mode 1

32 BIT DMA WORD (MODE 2) OR FRAME BUFFER OUTPUT WORD (MODE 3 OR 4)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	1	*	Control				Unit				Length				
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Serial Data Word															

NOTES: Length = 5 bit message length with bits 16-19 providing serial message length, coded n-1. Valid lengths are 1 to 16 bits, with bit 20 indicating a syllabized word.

TABLE 3-14. Input Message Format for Modes 2 through 4.

Bit 20 is set to **1** on all but the last syllable of syllabified words. This signal prevents the parity bit from being inserted on syllables of an output word.

Bits 21-24 (Unit) the rate programmable serializer is unit two.

Bit 25 is set to **1** when the serial output is LSB first.

Bit 26 is set to **1** when the input word is right-justified (MSB is bit 15).

Bit 27 is set to **1** to suppress parity on this word.

Bit 28 is set to **1** on the last word of a frame.

Bit 29 is not used.

Bit 30 & 31 select the serializer.

3.5.1.1 DMA Input Modes

Modes 1 and 2 described above are straightforward. In mode 1, the Serializer controls the rate at which it accesses data from the DMA as a function of the programmed bit rate. Messages are 16-bit only with two words per DMA transfer. In Mode 2 the data messages are variable length, and contain up to 16-bit words with message length, input justification, and output orientation encoded in each DMA message. The output rate will remain synchronous, assuming that the DMA channel provides data to the input FIFO at the rate required by the Serializer.

3.5.1.2 Frame Buffer Input with CVT Data

In **Mode 3** the Serializer operates asynchronously, outputting data whenever it receives a word (via its input FIFO) from the frame buffer memory. The FIFO forms a two word parallel register - the purpose of which is to insure a constant supply of data to the serializer with a minimum of sample delay. The serial output rate you select determines the word and frame transfer rate, by virtue of the rate at which the serial output rate accepts data from the frame buffer logic. The parallel input messages contain up to 16 bits of data, with message length, input justification, and output orientation coded in each message.

3.5.1.3 Frame Buffer Input with Reformatted Real Time Data

Mode 4 is more complex than modes 1-3. In mode 4 the Serializer accepts data from the frame buffer, which has buffered and reformatted two entire output frames with selected data from the input stream. The 32 bit output word has the same format as Mode 3, with the addition of an *End of Frame* flag that controls rate servoing. The frame buffer prepares the messages in the following manner. Each incoming DIT addresses a lookup table in the frame buffer memory. If you have selected the word to be included in the output frame, the memory supplies the word number in the output frame, and a bit to indicate if this word is the end of the PCM frame. Because the incoming data sources arrive asynchronously to the serial output words, an entire output frame is constructed before it is transferred into the serializer input FIFO. The Serializer extracts data from the FIFO at a rate determined by the Serializer's frequency synthesizer rate. The serializer attempts to hold the interval between output frame marks constant, and matched to the frame input rate. To do this, the serializer adjusts the synthesizer rate until it is extracting the frame mark word from the FIFO at the same time that the frame buffer completes the assembly of an input frame. In this context, the following frame mark is either *early, on-time* , or *late*. After the Serializer reads a frame mark from the frame buffer logic, it calculates a frequency correction, based on the number of bits serialized during the frame interval compared to the correct number of bits in a frame. The serializer frequency is adjusted to obtain an output frame rate that matches the input frame rate. The synchronizing technique requires that the buffer be able to hold more than a full frame of data, and the servoing system attempts to synchronize so that at frame mark time the buffer contains exactly two frames of data. However, the worst case rate mismatch (5% fast or slow) may require the buffer to hold up to three full frames before the correct output rate can be established.

3.5.2 Frame Rate Servo for Mode 4

The frequency synthesizer must be adjusted to produce an output bit rate that transmits a frame of data in the exact same time interval as an input frame. The synthesizer continuously adjusts the output frequency to maintain the phase relationship between the input and output frames (with a two frame delay). The frequency synthesizer is initially adjusted by an *early* or *late* detector to bring the frequency within the ±0.5% window. It does this by counting serialized bits during an input frame interval and testing to see if the output is within ±0.5% of the expected count. If the output count is not within the ±0.5% window, the output frequency is corrected by ±0.2%. Once the frame mark falls within the ±0.5% window, we enable a phase detector circuit that corrects the frequency ±0.1% each frame the phase error is greater than the previous frame.

3.5.3 Serializer Rate Register (Address 28)

This register controls the frequency synthesizer that in turn sets the Serializer bit rate. The eleven LSBs of the register contain a binary divisor that ranges from 973 to 1946 (decimal) to provide a two to one frequency change with 0.1% settability, thereby producing a 0.1% frequency accuracy figure, selectable from 16 to 32 MHz. The five MSBs of the register control a binary rate divider, with the divisor ranging from (2^0 to 2^{24}), thereby producing bit rates of from 32 MHz to 0.5 Hz.

Serializer Rate															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Binary Scale					Rate Divisor										

TABLE 3-15. Serializer Rate Register

The rate divisor must have a range of 973 to 1946, and is derived as follows:

$$RATE\ DIVISOR = \left[\frac{output\ \ frequency\ x\ binary\ scale}{16447.3Hz} \right]$$

The *Binary Scale* is the power of two that raises the input frequency to produce a frequency equal to or exceeding 16 million.

3.5.4 Serializer Control Register (Address 2A)

The control register enables the Serializer and selects the operating mode and output format controls as shown in TABLE 3-16.

Serializer Control Register	
Bit	**Function**
15-10	Six MSBs in Mode 4
9-7	Not used
6-5	PCM output code
4	Even parity
3	Enables parity
2-1	Serializer Mode Control
0	Enable

TABLE 3-16. Serializer Control Register

Bits 15-10 - are the 6 msbs of the Bits Per Frame register (Mode 4 only).

Bit 9 - set to **1** enables twice rate output clock: set to **0** enables bit rate output clock.

Bits 8, 7 - are not used.

Bits 6 & 5 - select the PCM output code as shown in TABLE 3-17.

Bit 4 - set to **1** enables Even parity; set to **0** enables Odd.

Bit 3 - enables parity (always trailing).

Bits 1 & 2 - are encoded to provide the following four operating modes:

Bit 1	Bit 2	Mode	Description
0	0	1	Fixed length, 16 bit DMA transfers.
1	0	2	Programmable-length DMA transfers.
0	1	3	CVT data from the frame buffer.
1	1	4	Data is from the frame buffer, and the serializer must synchronize the Serializer bit rate to a frame mark from the frame buffer.

PCM CODE SELECTION			
Bits		**Description**	
6	5	Serial PCM Code	
0	0	Read/Write	NRZ Level
0	1	Read/Write	Biphase Level
1	0	Read/Write	Biphase Mark
1	1	Read/Write	Delay Modulation Mark

TABLE 3-17. Serial Output PCM Code Selection

3.5.5 Bits Per Frame Register (Address 2C)

This register contains the 16 lsbs of the 22 bit word containing the number of bits per frame. The 6 msbs of this 22 bit word are in the 6 msbs of the Serializer Control register. The maximum frame length is 2,228,227 bits. Mode 4 uses the number of bits per frame to synchronize the *output rate* to the *input frame*.

3.5.6 0.5% Window (Address 2E)

This Mode 4 register contains the number of bits in 0.5% of the frame. The maximum value is 11,141 bits. This register forms a ±0.5% window at the end of frame that synchronizes the output rate to the input frame.

3.6 THE FRAME BUFFER

The frame buffer selects and formats data from the real time inputs to supply data in a time-division-multiplexed format to the rate-programmable serializer. The input data can come from the distribution input (via the distribution bus) or from an output device (0-3 & 7) via the A-bus.

The serializer accepts variable length messages up to 16 bits maximum. Input words over 16 bits must be syllabized into two output words for the serializer. Message formation to the serializer is complicated by the fact that the input structure data sources are providing variable length words (packed into a 16 or 32 bit format) that can be either left- (MSB) or right- (LSB) justified. Words greater than 16 but less than 32 bits will consist of a full 16 bit word and a 16 bit word containing the remaining bits. The location of the full and partial words in the input message is determined by the input word justification; left-justified words will contain a full word in the 16 MSBs and a partial word in the 16 LSBs, and right-justified words will be just the reverse.

The Word Selection Memory contains two control bits that perform the syllabization. The first bit indicates that the input word is greater than 16 bits, and the second indicates whether the serial output word is to be MSB or LSB first. The memory stores the two syllables with the first word (as addressed by the LSB of the Word Select Memory) containing the LSB of the input word (when the data is serialized LSB), then the MSB in the following word. When the serial output is MSB first, the first word contains the MSBs of the input word followed by the LSBs. The output word lengths for the two syllables output by the serializer must have the word length for each syllable calculated in accordance with the input word justification and the output word serialization (MSB or LSB). This information is provided to the serializer by the Output Control Word that accompanies the Serial Data Word.

The messages to the serializer are constructed in two separate formats depending upon the frame buffer mode. For *Asynchronous* input formats, selected input data from asynchronous sources is stored in memory as a current value table. The synchronous output format is produced by accessing the CVT in an output frame sequence as defined in a separate section of the frame buffer memory. The transfer rate of the output sequence is controlled by the word rate of the serializer. For *Synchronous* input formats, the selected input data is derived from synchronous input frames and stored in a programmable frame order with up to four frames of output data stored in memory. A word in the input stream defines the *end of frame*. At the completion of the second frame the output sequencer transfers the buffer to the serializer while the third buffer is being filled with input data. The output sequencer progresses sequentially through the four buffer memories thus providing a *rate buffer* for the serializer. The serializer uses the frame marks to servo the bit rate until output frames are synchronous to input frames with a two frame delay.

3.6.1 Frame Buffer Memory A32 Base Address (Address 02)

The frame buffer has a 4MB memory that is mapped in the VME memory space. The starting address of this memory is specified by the contents of the A32 Base Address Register. The memory is organized as 1MB by 32 bit words, accessible as 16 or 32 bits per transfer - i.e. it does not allow byte-wide transfers. Section 3.7 following explains how this memory is organized.

3.6.2 Frame Buffer Control Register (Address 20)

The frame buffer control register enables the transfer of data from the real time input streams through the frame buffer memory to the serializer input.

Bit 0 set to **1** to enable the synchronous input mode. in this mode selected data is reformatted into frame length buffers for serialization.

Bit 1 set to **1** to enable the asynchronous input mode. In this mode selected data is saved in a CVT memory and a frame description memory defines the output sequence.

Bit 2 is the fifth mask bit (extension of the Frame Buffer Mask register), that controls the use of ID bit 17 for data from device 0 (when using four word output).

3.6.3 Frame Buffer Mask Register (Address 22)

A bit in this register becomes an active masking bit when it is set to **1** ? set to **0**. ? The ID tags from the various input sources address a corresponding lookup table. These ID tags must be masked to provide the appropriately sized address. The distribution input always provides a 17 bit ID, and the DAC bus (device 7) always provides a 13 bit ID - and therefore do not require a mask. Devices 0 through 3 are normally processed data from the 505V PDSP card. The 505V card supports user-selected output formats providing ID sizes ranging from 12 to 17 bits. The mask register is provided to exclude the most significant bits from the ID word containing smaller ID tags. The mask register contains 16 bits that selectively mask bits 12 (LSB) through 15 (MSB) of the ID field on devices 0-3 (CVT). Device 0 can sometimes provide a 17 bit ID field, thus requiring a 5 bit mask. The fifth mask bit, controlling this 17th ID bit, is in the Control Register.

Digital Device 0-3 Mask Registers															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MSB ←			→ LSB	MSB ←			→ LSB	MSB ←			→ LSB	MSB ←			→ LSB
Device 0				Device 1				Device 2				Device 3			

TABLE 3-18. Digital Device 0-3 Mask Registers.

3.6.4 Frame Interval Register (Address 24)

The Frame Interval Register controls a “watch dog” timer that is set to the frame interval plus 10%, and controls the serializer when the input source loses synchronization. This feature is only used with a synchronous input (Mode 4). The counter is preset to the value specified by the 14 LSBs of the register, and counts microseconds, milliseconds, or seconds as specified by the two MSBs of the register. If the counter reaches zero before the next frame mark is received, a *Sync Lost* flag is set. The frame buffer will send any data remaining in the current frame buffer, then stop outputting data to the serializer until two complete frame buffers have be re-acquired. The serializer input FIFO will go empty, causing the serializer to output a complimenting one/zero pattern until the frame buffer regains sync, and normal serialization can resume. The rate selection bits are as follows.

Counter Rate Selection		
Bits		**Description_**
15	14	
0	0	Disable Interval Count
0	1	Count Microseconds
1	0	Count Milliseconds
1	1	Count Seconds

TABLE 3-19. Interval Counter Rate Selection

3.7 FRAME BUFFER MEMORY ORGANIZATION

3.7.1 Synchronous Input Mode

Memory allocations are shown in TABLE 3-20. The memory is divided into two 512kx32-bit word sections. The lower half performs word selection by acting as a lookup table addressed by the input DIT, and the upper half provides the frame buffers. Data selected for serialization can come from the distribution input (which provides a 17 bit ID tag) or from devices 0, 1, 2, 3, or 7 on the A-bus. Device 0 supports a 17 bit ID; Devices 1, 2, and 3 support 16 bit ID tags. Device 7 sends data to the DACs and has a fixed 13 bit ID tag.

SYNCHRONOUS MODE MEMORY ALLOCATIONS				
	0000 →		31 ←	→ 0
Frame	512kB **80000 →**	Device 0 (128k x 32)	4 Control Bits	17-bit Address
Buffer	256kB **88000 →**	Device 1 (64k x 32)	"	"
Word	256kB **100000 →**	Device 2 (64k x 32)	"	"
Select	256kB **108000 →**	Device 3 (64k x 32)	"	"
Memory	256kB **180000 →**	Device 7 (64k x 32)	"	"
	512kB **200000 →**	Dist. Input (128k x 32)	"	"
Frame	512kB **280000 →**	Frame Buffer 1 (128k x 32)	15 Control Bits	16-bit Word
Buffer	512kB **300000 →**	Frame Buffer 2 (128k x 32)	"	"
Memory	512kB **380000 →**	Frame Buffer 3 (128k x 32)	"	"
	512kB **400000 →**	Frame Buffer 4 (128k x 32)	"	"

TABLE 3-20. Synchronous Mode Memory Allocations

3.7.1.1 Word Selection Memory

The word selection memory is partitioned to provide two 128k x 32-bit word lookup tables for Device 0 and the distribution input data, and four 64k x 32-bit word lookup tables for devices 1, 2, 3, & 7. The input data ID tags are appropriately masked, and then address the corresponding lookup table in the word selection memory to determine if (1) the word is marked for inclusion in the frame buffer, and (2) the position of the word in the output frame. The least significant 17 bits of the 32-bit word form the address in the output frame, and 4 bits of the word provide control as shown in TABLE 3-21.

FRAME BUFFER WORD SELECT CONTROL BITS	
Bit	**Function**
29-31	Not used
28	End of frame
27	Save the word
26	Not used
25	Serial output is LSB
21-24	Not used
20	Output word is greater than 16 bits
17-19	Not used

TABLE 3-21. Control Bits in Frame Buffer Word Select

Bit 28 is set to 1 to indicate that the current input word is the last word in the current frame buffer.

Bit 27 is set to 1 to save the current input word in the current frame buffer at the relative address (32 bit word address) supplied by bits 0 through 16.

Bit 25 is set to 1 when the data is to be serialized LSB first. This bit is used when the input word is longer than 16 bits (bit 20 set to 1) the word must be stored in the frame buffer as two 16 bit words. When the serial data is output LSB first, the least significant 16 bit word is stored first followed by the most significant word. When the output is MSB first, the most significant 16 bit word is stored first followed by the least significant word

Bit 20 is set to 1 when the input word is greater than 16 bits and must be syllabized into two 16 bit words.

3.7.1.2 Frame Buffer Memory

The upper 512kx32-bit words are divided into four 128kx32-bit *frame buffer memories*. The four memories form a circular buffer. Two full frames must be buffered before the serializer will start. A third buffer is normally filled while the first buffer is being output. Since the incoming data rate may vary as much as ±5% of the expected (programmed) rate, and the rate error is cumulative during the rate servoing time, the input and output frames can slip by as much as 70% before the output stabilizes to the correct rate. When the programmed rate is faster than the input rate, the serializer will temporarily output a buffer in less time than it takes to fill the next input buffer. At this time, the serializer will be unloading the second frame buffer before the next input buffer is complete. Since the input buffer is filled in random order, data cannot be output until the buffer is complete, thus requiring a second full frame buffer to properly synchronize the two rates.

When the output sequencer reads data from the output buffer, the 16 LSBs contain the output word. The sequencer uses fifteen control bits from the upper word to provide information to the serializer. These control bits are shown in TABLE 3-22.

OUTPUT WORD CONTROL BITS	
Bit	**Function**
31	Must be 0
30	Must be 1
29	Not used
28	End of frame
27	No parity on this word
26	Input word is left-justified
25	Serial output is LSB
24-21	Unit = 2
20	Syllable of output word
16-19	Serial word length

TABLE 3-22. Control Bits in the Frame Buffer Output Word

Bits 31 & 30 select the serializer.

Bit 29 is not used.

Bit 28 is set to 1 on the last word of a frame.

Bit 27 is set to 1 to suppress parity on this word.

Bit 26 is set to 1 when the input word is right-justified (MSB is bit 15).

Bit 25 is set to 1 when the serial output is LSB first.

Bits 24-21 the rate programmable serializer is unit two.

Bit 20 is set to 1 on all but the last syllable of syllabified words. This signal prevents the parity bit from being inserted on syllables of an output word.

Bits 19-16 are the serial word length. Valid lengths are 1 to 16 bits. The length field is coded n-1.

3.7.2 Asynchronous Input Mode

The memory allocations are shown in TABLE 3-23. The memory is divided into two 512kx32-bit word sections - with the lower half used for word selection (similar to the word selection memory for synchronous input mode) and providing an address to a current value table located in the last 32k word block of the frame description memory, which stores the last value of the real time input data, thus forming a current value table. The input data ID tags are masked to the proper length using the contents of the frame buffer mask register as explained in section 3.6.3. The remaining portion of the upper half of the memory provides a 480k word table that describes the order in which the CVT data from the upper 32k word block is to be sent to the serializer to construct an output frame.

ASYNCHRONOUS MODE MEMORY ALLOCATIONS				
		Bits →	31 15	14 0
	0000 →			
CVT	512kB	Device 0 (128k x 32)	3 Control Bits	15-bit CVT Address
	80000 →			
	256kB	Device 1 (64k x 32)	"	"
	88000 →			
Word	256kB	Device 2 (64k x 32)	"	"
	100000 →			
Select	256kB	Device 3 (64k x 32)	"	"
	108000 →			
	256kB	Device 7 (64k x 32)	"	"
Memory	**180000 →**			
	512kB	Dist. Input (128k x 32)	"	"
	200000 →			
Output Frame Descr. Memory	1920kB	(480k x 32)	1 Control Bit	"
	3E0000 →			
CVT Memory	128kB	(32k x 32)	15 Control Bits	16 Data Bits
	400000 →			

TABLE 3-23. Asynchronous Mode Memory Allocations

3.7.2.1 CVT Word Select Control Bits

When bit 27 is a 1, the 15 lsbs of the CVT Word Select memory provide the CVT address at which the data is saved. If bit 20 is a 0 the 16 lsbs of the data are saved. If bit 20 is a 1, the word is saved as two 16 bit syllables. If bit 25 is a 1, the 16 lsbs are stored at the CVT address and the 16 msbs at the next address. If bit 25 is a 0, the 16 msbs are stored at the CVT address and the 16 lsbs at the next address. The control bits are shown in TABLE 2-24.

CVT WORD SELECT CONTROL BITS	
Bit	**Function**
31-28	Not used
27	Save the word
26	Not used
25	Serial output is LSB
24-21	Not used
20	Output word is greater than 16 bits
19-17	Not used

TABLE 3-24. Three Control Bits in CVT Word Select

Bit 27 is set to 1 to save the current input word in the current frame buffer at the relative address (32 bit word address) supplied by bits 0 through 16.

Bit 25 is set to 1 when the data is to be serialized LSB first. This bit is used when the input word is longer than 16 bits (bit 20 set to 1) the word must be stored in the CVT memory as two 16 bit words. When the serial data is output LSB first, the least significant 16 bit word is stored first followed by the most significant word. When the output is MSB first, the most significant 16 bit word is stored first followed by the least significant word

Bit 20 is set to 1 when the input word is greater than 16 bits and must be syllabized into two 16 bit words.

3.7.2.2 CVT Frame Description Memory

The frame description memory starts at 0x200000 and provides up to 491520 words of output frame description. The memory provides a 15 bit CVT memory address in the 15 lsbs and an “end of frame” flag in bit 28. When a word is read with bit 28 set to **1**, the frame address counter is preset to 0x200000 to start the next frame.

3.7.2.3 CVT Data Memory

The 32k word CVT memory contains a 16 bit data value in the 16 lsbs and a 15 bit control word that is identical to the frame buffer output control word shown in TABLE 3-22 above.

3.8 ASYNCHRONOUS DATA OUTPUT FEATURE

The Asynchronous Data output feature permits you to transmit arbitrarily selected data from the TDP data stream to up to four standard asynchronous data channels (with programmable properties) plus one additional fixed rate, fixed format channel. The standard configuration of the card uses differential (RS-485) drivers.

The asynchronous channel data is sent as messages to device 5. The unit address field (bits 21-24) must be set to C,D,E, or F, with the two lsbs (21 & 22) equaling the value written to the Asynchronous Channel Select register (Address 34). The channel that is to receive the data is selected by the function field (bits 16-20), with the six messages encoded in bits 16-18. The message formats are shown in TABLE 3-38 on page 3-39.

3.8.1 Asynchronous Channel Control Registers (Address 30 AND 32)

The registers at addresses 30 and 32 establish word properties for Asynchronous Channels one through four. Channels five and six are reserved to form a special serial channel that transmits a fixed rate (368.64 KHz) 24-bit message. The contents of the control registers are shown in the tables below.

Channels 2 & 4			**Channels 1 & 3**		
15 14 13	12 11 10	9 8	7 6 5	4 3 2	1 0
Rate	Parity	Length	Rate	Parity	Length

Bits			Function
7/15	**6/14**	**5/13**	**Baud Rate**
1	1	1	153.6K
1	1	0	76.8K
1	0	1	38.4K
1	0	0	19.2K
0	1	1	9.6K
0	1	0	4.8K
0	0	1	2.4K
0	0	0	OFF
4/12	**3/11**	**2/10**	**Parity**
1	1	1	Space Parity
1	1	0	Mark Parity
1	0	1	Odd Parity
1	0	0	Even Parity
0	-	-	No Parity
-	**1/9**	**0/8**	**Length**
-	1	1	7 bits, 2 stop bits
-	1	0	7 bits, 1 stop bit
-	0	1	8 bits, 2 stop bits
-	0	0	8 bits, 1 stop bit

TABLE 3-25. Asynchronous Channel Control Registers

3.8.2 Asynchronous Channel Select Register (Address 34)

The Asynchronous Channel Select Register sets the unit address for the asynchronous channels on the SIMR card. The channel select register allows up to four cards to be installed in a single system. The *Unit Select* field (bits 21-24) in the messages to Device 5 must be set to Units C-F to select a Reconstructor card. Bits 23 & 24 must be set to 1 to select an asynchronous channel, and bits 21 & 22 must match the value written to the two lsbs of the Asynchronous Channel Select register for you to use the asynchronous channels on that card. The table below shows the value to be written to bits 1 and 0 of the Channel Select Register to correspond with the *Unit Select* field of a message. The message formats for the asynchronous channels are shown in TABLEs 3-38 & 3-39.

Unit Select	Bit 1	Bit 0
C	0	0
D	0	1
E	1	0
F	1	1

3.9 SYNCHRONOUS TRANSMIT CHANNELS

The *Synchronous Transmit* channels allow you to transmit the telemetry data prepared by the frame buffer over multiple low rate communication channels rather than being serialized into a single high rate channel by the data serializer. You can programmably select to transmit the telemetry frames over a single channel, or fanned across up to six channels. Each telemetry record consists of a 50 bit preamble message that contains a 24 bit synch pattern, 3 bit number of channels, 7 bit record count, and a 16 bit number describing the number of bits in the TM message. The preamble is followed by the TM frame, which can contain up to 65520 bits. The record is then ended by a 16 bit CRC word for message verification. A variable length fill message of alternating ones and zeros is sent following the CRC word, and is terminated by the synch pattern of the next telemetry record. The synchronous channels provide a 64k-bit frame buffer memory for each channel, as well as the additional logic required to process the variable length, variable orientation input data from the frame buffer memory into a processed telemetry frame. The telemetry frames are formatted into *telemetry records* (with preamble and CRC) that are transmitted by the serial output channels. Consecutive TM frames are transmitted on sequential output channels. The data is recovered by a synchronous receive card that merges the TM frames into a single serial output. The telemetry frame is generated by the frame buffer memory using the same software used for the rate-programmable serializer. The synchronous output channels generate a rate-programmable clock, or can be programmably selected to use an external clock. Software is provided to select the synchronous output and specify the number of active output channels.

3.9.1 Transmitter Control Register (Address 38)

Transmitter Control Register		
Bits	**Description**	**Mode**
5-3	Selects the number of active channels	
2	Even parity	
1	Enable parity	
0	Enable transmitters	

TABLE 3-26. Transmitter Control Register

Bits 5-3 - select the number of active channels, where 0 selects one channel and 7 selects eight channels. This value is transmitted as part of the preamble message.

Bits			*Function*
5	*4*	*3*	
0	*0*	*0*	*1 Channel*
0	*0*	*1*	*2 Channels*
0	*1*	*0*	*3 Channels*
0	*1*	*1*	*4 Channels*
1	*0*	*0*	*5 Channels*
1	*0*	*1*	*6 Channels*
1	*1*	*0*	*7 Channels*
1	*1*	*1*	*8 Channels*

Bit 2 - is set to **1** to generate even parity and set to **0** for odd.

Bit 1 - is set to **1** to include parity in the data, and set to **0** to exclude it.

Bit 0 - is set to **1** to start the transmission of data. If no data has been loaded, then a fill pattern of alternating ones will be output on all active channels.

3.9.2 Channel Selection (Address 3A & 3C)

The output mapping registers control the physical to logical placement of the eight channels. The hardware fans the PCM frames sequentially to the number of physical channels enabled. The number of active channels must match the number of channels specified in the control register at address 38. The logical channels must start at zero and count up sequentially to the number of enabled channels. The numeric value of the last logical channel will equal the number of active channels in bits 3, 4, & 5 of the transmitter control register.

Channel Selection 1-4		
Bits	**Description**	**Mode**
15	Physical Ch 4 enable	W
15	Physical Ch 4 carrier detected	R
14-12	Physical Ch 4 logical channel	R/W
11	Physical Ch 3 enable	W
11	Physical Ch 3 carrier detected	R
10-8	Physical Ch 3 logical channel	R/W
7	Physical Ch 2 enable	W
7	Physical Ch 2 carrier detected	R
6-4	Physical Ch 2 logical channel	R/W
3	Physical Ch 1 enable	W
3	Physical Ch 1 carrier detected	R
2-0	Physical Ch 1 logical channel	R/W

TABLE 3-27. Channel Selection - 1-4

Channel Selection 5-8		
Bits	**Description**	**Mode**
15	Physical Ch 8 enable	W
15	Physical Ch 8 carrier detected	R
14-12	Physical Ch 8 logical channel	R/W
11	Physical Ch 7 enable	W
11	Physical Ch 7 carrier detected	R
10-8	Physical Ch 7 logical channel	R/W
7	Physical Ch 6 enable	W
7	Physical Ch 6 carrier detected	R
6-4	Physical Ch 6 logical channel	R/W
3	Physical Ch 5 enable	W
3	Physical Ch 5 carrier detected	R
2-0	Physical Ch 5 logical channel	R/W

TABLE 3-28. Channel Selection - 5-8

3.9.3 Transmit TM Frame Size (Address 3E)

This register contains the number of bits per data frame (excluding preamble and postamble messages). The value is loaded as n-1. The value can range from 1,000 to a maximum of 65,528 bits per data frame. This value is transmitted as part of the preamble message.

Transmit Frame Size		
Bits	**Description**	**Mode**
0-15	Bits per frame	R/W

TABLE 3-29. Transmit Frame Size

3.9.4 Record Format

Each telemetry record consists of a 50 bit preamble message that contains a 24 bit sync pattern (FAF320), number of active channels (in n-1 notation), frame number, and number of bits in the TM message. The preamble is followed by the TM frame and the record concludes with a 16 bit CRC word for message verification.

3.10 Inertial Navigation System Control Register (Address 36)

This register enables INS message inputs and provides a programmable offset for ID tag generation.

INS Control Register															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
E	Unused						← ID Offset →								

TABLE 3-30. INS Control Register

Bit 15 is set to **1** to enable INS messages.

Bits 0 through 8 form a user-entered ID field containing the nine msbs of the 17 bit ID tag.

INS messages are received as serial 32 bit packets containing an eight bit ID word, a 23 bit data word, and a parity bit. The INS control register provides the INS input enable control and a user-specified nine bit ID *page control.* When enabled, INS messages are first arranged into a 64 bit format, then input to the distribution system by outputting the messages to the A-bus, where they are directed to the feedback port. The feedback port places the messages on the input bus where they are time-tagged and processed by the distribution in the same manner as PCM input words. The feedback message is shown in TABLE 3-36. The *ID* portion of the message is formed by combining the eight bit INS ID tag (lsbs) and the nine user-supplied ID bits (msbs) to generate a 17 bit ID tag. The INS *data message* is a 24 bit data word with the MSB a *Parity* bit. Data parity is tested and if an error is detected the parity error flag (bit 51) is set to **1**. The next two bits are encoded and indicate *Polarity*, *Test Data*, or *Data Not Available.* The decoded sign plus the 21 bits of data form a 22-bit data message. This is left-justified in the 32-bit data field so that the data becomes a 32-bit, 2's complement, binary fraction. This is consistent with the default management of LONG data in the telemetry data processor. *Test Mode* and *Data Not Available* are decoded to form two unitary indicator bits, and occupy the two LSBs of the data field. Messages received in Test Mode have the LSB (bit 0) set to **1** in the output data word and messages indicating Data Not Available have bit 1 set to **1** in the output message.

First ID Word															
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
0												pe	0		uid
Second ID Word															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
uid continued...								INS id							
First Data Word															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
s	Data														
Second Data Word															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Data														dna	tm

TABLE 3-31. INS Message Format

LEGEND: 0 = not used; pe = parity error; uid = user id; dna = data not available
s = sign; tm = test mode

3.11 PROGRAMMING CONSIDERATIONS

The Model 512VA contains a programmable Time Base Generator that can insert a time base into the data stream, thereby allowing reconstruction of the recorded data. The PDSP can pass under program control interval time data with bit 13 of the ID word set. The 512VA can insert three time-of-year 64-bit messages directly into the output stream to Device 0, the Host Interface.

The card has six transmit only asynchronous channels implemented as an extension of *Device 5* (Serializer), on the A-bus. The system supports up to four 512VA cards and the *units* field of the ID word (values C through F) selects the desired serializer group. Three LSBs of the ID word *Function* field select the channel number. For channels 1 through 4, data comes from the 7 or 8 LSBs of the data word. Channels 5 and 6 are combined to form a special 24-bit serial channel. Messages to the hardware Reconstructor are transferred via the DMA channel. Reconstruction information must be encoded in the ID field as shown in the tables below. Bits 30 & 31 select the A-bus device that will receive the reconstructed data as follows:

BITS 31	BITS 30	OUTPUT	DESTINATION
1	1	= Device 7	- DAC Bus
1	0	= Device 4	- Feedback Port
0	1	= Device 5	- Serializer
0	0	= Device 0	- DMA Channel

TABLES 3-32 through 3-35 show the data format as the Reconstructor will read it from memory via the DMA. TABLES 3-36 through 3-39 show Reconstructor output message formats to the A-bus.

3.11.1 Messages to Device 7 - DAC & Discrete Words

<table>
<tr><th colspan="16">ID (MSH Word)</th></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>1</td><td>1</td><td>T</td><td>1</td><td>S2</td><td>S1</td><td colspan="10">Address</td></tr>
<tr><th colspan="16">Data (LSH Word)</th></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>09</td><td>08</td><td>07</td><td>06</td><td>05</td><td>04</td><td>03</td><td>02</td><td>01</td><td>00</td></tr>
<tr><td></td><td colspan="15">← 1 Bit Word</td></tr>
<tr><td colspan="8">8 Bit Word</td><td colspan="8"></td></tr>
<tr><td colspan="16">16 Bit Word</td></tr>
</table>

TABLE 3-32. Discrete Word Format

LEGEND: Bits 31=1 & 30=1 for Device 7, T = Time Interval Tick
Bit 28 = **1** for Discrete
S2 = **1** for 16-bit word, S1 = **1** for 8-bit word, S1 & S2 = **0** for 1-bit word
10 bits define the Discrete Address for 1024 Discrete lines.

ID (MSH Word)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	T	0	Address											
Data (LSH Word)															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	12-Bit 2's Complement											not used			

TABLE 3-33. DAC Word Format

LEGEND: Bits 31=1 & 30=1 for Device 7, T = Time Interval Tick, Bit 28 = **0** for DAC
12 bits define the Address for 4096 Analog channels
S= Sign bit of 12-bit, 2's complement data word.

3.11.2 Reconstructor Messages to Device 5 - Serializers & Misc.

The Reconstructor uses *Device 5 Units C-F* to send data via the asynchronous channels. The two msbs of the *unit* field must be set to **1** and the two LSBs of the *Unit Select* field select the Reconstructor card. (See the description of the Asynchronous Channel Select Register.) The three LSBs of the *Function* field select the output channel. Channels 1-4 are 7 or 8 bit channels. We use channels 5 & 6 to form a 24-bit serial word.

Device 5 Unit 0 is a NO-OP, *Device 5 Units 1 and 2* are bit length programmable serializers, with unit 1 being a fixed rate serializer on the 504VA DIST card, and unit 2 a programmable rate serializer on the 512VA SIMR card. The programmable rate serializer is not accessible from the A-bus. Input data is formatted by a frame buffer memory or may be input by the reconstructor DMA channel. This serializer supports syllabified words and programmable msb/lsb output.

Data to the fixed rate serializer must be MSB-justified as it is serialized from bit 15. The number of bits for serialization is specified as n-1 (0 to 15) in the *function* field. Data to the asynchronous channels is either 7 or 8 bits, LSB-justified in the data field, or an 8-bit tag and 16-bits of data which are combined to form the 24-bit message. Invalid OP-code provides a 16-bit ID tag. *Device 5 Unit 8* is the Invalid OP-code register. (The algorithm firmware uses the Invalid OP-code register to send an interrupt to the host when the firmware decodes an illegal OP-code. You should not address Device 5 Unit 8).

The word formats for data sent to the Reconstructor are shown below.

ID Word															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	1	T	Control				Unit Select				Function				
Data Word To Serializer															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
msb															lsb
Data Word To Asynchronous Channels 1 - 4															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
								msb		←7 or 8 bit data→					lsb
First Data Word To 24-Bit Asynchronous Serial Output (Channel 5)															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
								Eight Bit ID Tag							
Second Data Word To 24-Bit Asynchronous Serial Output (Channel 6)															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
16-Bit Data															
Data Word For Invalid OP-code															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
16-Bit ID Tag															

TABLE 3-34. Device 5 Word Format

LEGEND: Bits 31=0 & 30=1 for Device 5, T = Time Interval Tick

Bits 25-21 apply only for the programmable rate serializer.

```
Bit 25 = Output LSB
Bit 26 = Input is right-justified
Bit 27 = No parity
Bit 28 = End of frame
```

3.11.3 Messages to Device 4 - Feedback Port

Sending data to the Feedback port from the Reconstructor lets us use the PDSP to perform scaling or other modification of the data.

ID (MSH Word)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	0	T	ID Tag												
Data (LSH Word)															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	Data														

TABLE 3-35. Feedback Word Format

LEGEND: Bits 31=1 & 30=0 for Device 4, T = Time Interval Tick, 13-bit ID field
S = Sign Bit, 16-bit 2's compliment Data word.

3.11.4 A-Bus Messages to Device 4 - Feedback Port

The Reconstructor maps data destined for the Feedback port into a 64-bit DIT, output via the A-bus to Device 4, formatted as shown in the following table.

First ID Word															
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
0															
Second ID Word															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ID															
First Data Word															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Sign Extension															
Second Data Word															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
S	Data														

TABLE 3-36. A-bus Message Format for the Feedback Port

LEGEND: First ID word is all 0
Offset bits 47-45 of the ID word are selected in the Reconstructor Control Register
S = Sign bit is used to fill bits 31-16

3.11.5 A-Bus Messages to Device 5 - Serializers & Misc.

Messages to Device 5 contain a 5-bit *Function* field, which varies with the specific unit, and a 4-bit *Unit Select* field, which allows 16 different TDP functions to share Device 5, as shown in TABLE 3-36.

Unit 1 is a bit-length-programmable serializer that is part of the 504VA DIST card. This Serializer outputs data from the A-bus at a clock rate of 16 MHz. Unit 2 is the rate-programmable serializer, with one Serializer per 512VA SIMR card. This serializer receives input from either the frame buffer logic or the reconstructor DMA, and cannot be controlled directly from the A-bus. The fixed rate serializer accepts bits per word (coded as n–1) in the four LSBs of the *Function* field, thereby providing word lengths of 1 to 16 bits. The bits per word control is in the four LSBs of the most significant 16-bit word and the data is most significant bit justified in the least significant 16-bit word of the A-bus transfer.

ID Word															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Not Used							Unit=1				Word Length n–1				
Data Word															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MSB Justified Data															

TABLE 3-37. A-bus Message Format for the Serializer

3.11.6 A-Bus Messages to the Invalid OPcode Register

The *Invalid OP-code* message also shares Device 5. This message is assigned Unit 8, and the Function bits are not used. The second word of this message contains the ID of the source that called the invalid OP-code.

3.11.7 A-Bus Messages to the Asynchronous Serial Channels

The asynchronous channels use Device 5 *Units C-F*, each of which selects a Reconstructor card corresponding to the value written to the Asynchronous Channel Select Register (address 34). The *Function* field determines over which of the 6 asynchronous channels on the card you transmit your data. For channels one through four the data is LSB-justified in the second word of this message, with the 7 or 8 bit word being serialized MSB first. The message format is shown in TABLE 3-37.

ID Word															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Not Used							Unit=C-F				Channel=1-4				
Data Word															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
								msb	←7 or 8 Bit Data→						lsb

TABLE 3-38. A-bus Message Format for 7 or 8 Bit Serial Channels

Channels 5 and 6 are combined to provide a special 24-bit word with 8 bits of ID and 16 bits of data. A word sent to channel 5 is saved with the eight LSBs used as the ID tag for the 24-bit message. The channel 6 word following the ID contains a 16-bit data word. The resulting 24-bit word is then serialized, with the LSB of the *data* word being sent first. The message format is shown in TABLE 3-38 below.

First ID Word															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Not Used							Unit=C-F				Channel=5				
First Data Word															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
								8-Bit Data							
Second ID Word															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Not Used							Unit=C-F				Channel=6				
Second Data Word															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
16-bit Data															

TABLE 3-39. A-bus Message Format for 24-Bit Serial Channel

3.11.8 Rate Programmable Serializer

The 512VA provides an optional programmable serializer that only functions under software control. The serializer operates in four modes and serializes data from either the “real time input stream” or from a stored data file. In modes one and two, the serializer receives data from the reconstructor DMA channel in the form of a 32 bit word. Mode one provides a fixed 32 bit word length serialized msb first. Mode two provides variable word length, input justification, and msb or lsb output serialization. You can select trailing parity. The 16 msbs of the input word contain the control fields and the 16 lsbs provide the data that can be right- or left-justified. The input message format is shown in TABLE 3-38, and is the same for modes two, three, and four. Modes three and four receive their input words from the frame buffer memory, which extracts selected data from the real time inputs. Modes one, two, and three output data at the programmed rate. Mode four servos the programmed output rate to match a synchronous input frame rate. The servo function requires the program to supply a 22 bit word containing the number of bits per frame. This word consists of 16 bits in register 2C, and 6 msbs in register 2A. The bits per frame count must include the parity bits if the format includes parity. The servo also requires a program generated word that equals the number of bits in ±0.5% of a frame.

3.11.9 Frame Buffer Memory

The frame buffer memory operates in two modes. In the *asynchronous* mode the serializer is in mode three. The frame buffer memory is divided into two sections, with half serving as a *data source selector,* and the other half providing an *output frame description* and a 32k word *current value memory*. The selection memory is arranged to provide six segments that are addressed by the ID tags of the distribution input data and digital devices 0, 1, 2, 3, and 7 on the A-bus. The 15 lsbs of the memory provide an address, in the CVT section, where you can store selected data. The upper 16 bits (shown in TABLE 3-14) provide three control flags. The control flags select the word for output, and handle the syllabizing of input words exceeding 16 bits.

The frame description memory is addressed sequentially to provide a user-defined output frame. The program must include the PCM synchronization pattern and subframe synchronization words in the CVT memory. The frame description memory provides the CVT address for each word of the output frame and a *last word* flag that presets the address to the start of the frame description memory.

The 16 lsbs of the 32k word CVT memory provide a word or syllable of a word that can be from 1 to 16 bits long, and can be right- or left-justified in the data field. The 16 msbs provide control fields (as shown in TABLE 3-14) that establish the serial word length, word syllabizing for parity generation, parity control, input and output word orientation, a four bit unit select field that must be set to select unit two, and bit 30 must be set to **1** and bit 31 set to **0** to select the serializer.

The frame synchronous mode uses the serializer in mode four (the serializer servos the bit rate to a frame rate pulse). The first half of the memory is organized as for the CVT mode, but provides a 17 bit address that establishes the word position in the 64k word output frame buffer. The upper half of the memory is divided into four frame buffers, which are output sequentially to form a ring buffer. The PCM synchronization pattern and any constant data, as well as the control words that are provided by the program must be stored in all four buffers. When enable, the frame buffer operates as follows.

The selection memory is arranged to provide six segments that are addressed by the ID tags of the distribution input data and digital devices 0, 1, 2, 3, & 7 on the A-bus. The 17 lsbs of the memory provide an address in the currently active frame buffer (one of four) in the upper section of memory where you want to store selected data. If the control word in the currently addressed selection memory indicates that the input word is greater than 16 bits, the word is syllabified with the first syllable stored in the 16 lsbs of the specified address and the second syllable stored in the 16 lsbs of the following memory location. The first syllable will contain the 16 lsbs of the data word when the serial data is lsb first, or the 16 msbs when the serial data is msb first. The data is stored in the 16 lsbs of the frame buffer memory using a *read/modify/write* cycle to preserve the content of the control word in the 16 msbs. When the addressed selection memory has the *end of frame* flag set to **1**, the word is stored in the specified location of the output buffer memory, and that buffer is queued to be unloaded by the output sequencer. The next buffer is selected as the current write buffer into which the next frame of data will be formatted. The output sequencer cannot start transferring data to the serializer until two frame buffers have been filled. The frame interval counter, in this mode, resynchronizes the output buffers when the input has lost synchronization and returned to Search. When the interval timer times out, the frame buffer completes the transfer of any finished buffers, but must then wait for two complete input frames before it can resynchronize data transfers to the serializer.

3.11.10 INMARSAT Data Link Transmitter

The synchronous channels transmit data from the frame buffer memory via one to eight synchronous modulators. When the data is spread across multiple channels each channel transmits a record containing a preamble, one telemetry frame, and a CRC word. The data is spread across program-specified logical channels with the program making the physical to logical assignments in the appropriate channel select registers (Address 3A & 3C). Only 6 physical channels are available when using the INS inputs. The input data must be supplied at a rate that allows the message (including 66 bits of overhead for each frame) to be transmitted as well as a fill block which separates adjacent frames. The fill block should be from one to ninety five percent of the record to accommodate variations in the input and transmit rates. The word transmission rate is controlled by the data serializer output bit rate (Address 28) with the serializer programmed to asynchronous frame mode. The serializer bit rate is determined by the following equation:

$$Transmit\ Frame\ Rate = \left[\frac{1}{TBR}\right] \times [\ BPF + 66 + FILL\ ]$$

TBR = Transmit Baud Rate (4800, 9600, 19200)

BPF = Bits Per Frame

FILL = 1% to 95% of bits per frame

$$Serial\ Bit\ Interval = \left[\frac{TFR}{BPF \times NOC}\right]$$

NOC = Number Of Channels being transmitted

$$Serial\ Bit\ Rate = \left[\frac{1}{SBI}\right]$$

The program must select the number of output channels, the physical to logical assignment of each channel, and the number of bits in the TM frame.

3.12 DAC BUS INTERFACE

The DAC Bus interface transfers data from the TDP to the DAC converters and discrete line circuits such as our Model 2240 chassis. Device 7 is supported with special algorithms for analog and discrete line outputs - and to provide the required message format. The hardware interfaces the device bus to the DAC bus, which captures ID and Data addressed to Device 7. The data consists of a 16 bit word, while the ID word contains 12 address lines plus four lines that configure the receiving hardware. These 32 lines, along with three control signals, are buffered and brought to the J2 (RC2 on schematics) connector of the 512VD-40 or 512VE-50 cards. The pin numbers and signal functions are listed in TABLE 2-13 of Section 2.

Switch selectable speeds allow transfers from 0.8 to 2.2 megawords per second. FIGURES 3-40 and 3-41 contain the timing diagrams for high and low rate transfers. A word transfer is initiated by the Digital to Analog Address Enable signal 9DACAEB, which is set to **0** when the address is output on the bus. The external hardware can extend the transfer cycle by setting WAIT signal 9DACWAT to **0** if the external device is not ready for the data word. When wait is set to **1** the data strobe signal 9DATSTB will be set to **0** to complete the data transfer cycle.

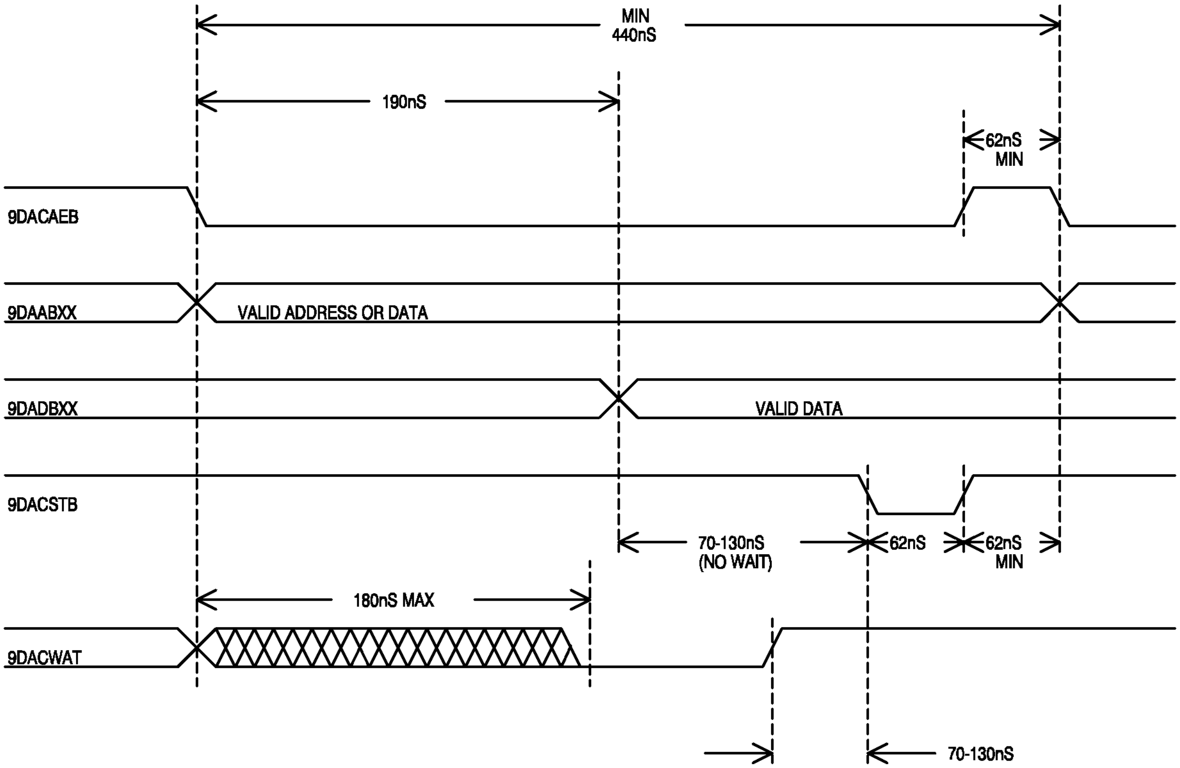


FIGURE 3.1 (FAST CYCLE)

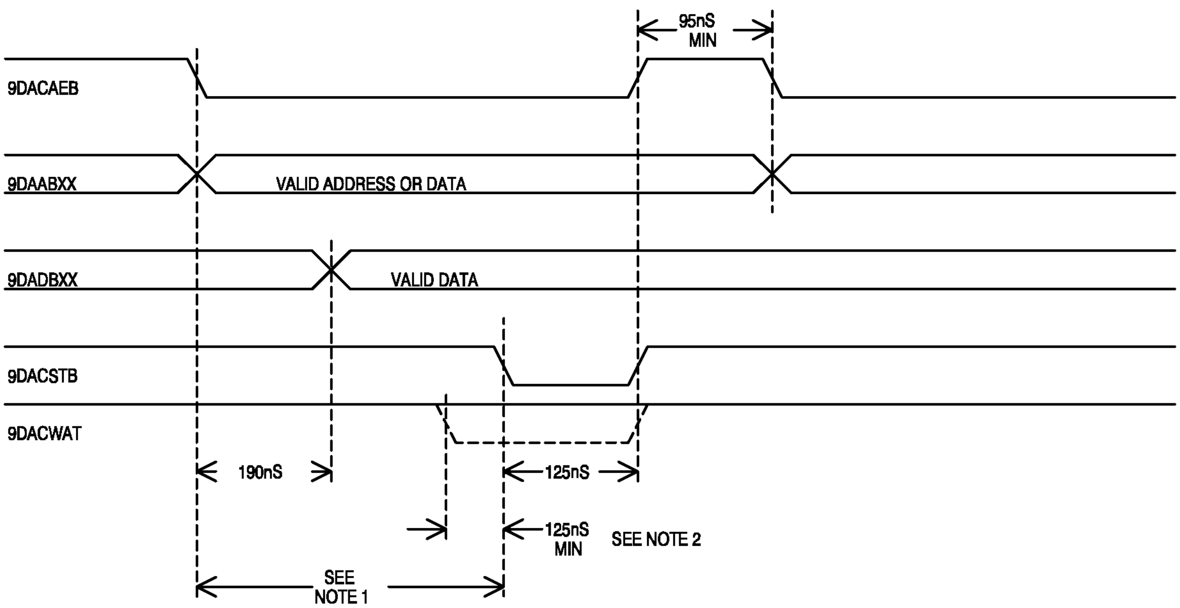


FIGURE 3-41 DAC BUS TIMING (SLOW CYCLES)

NOTES: 1) SWITCH SELECTABLE DELAY:
2) WAIT IS SAMPLED AT END OF DELAY.

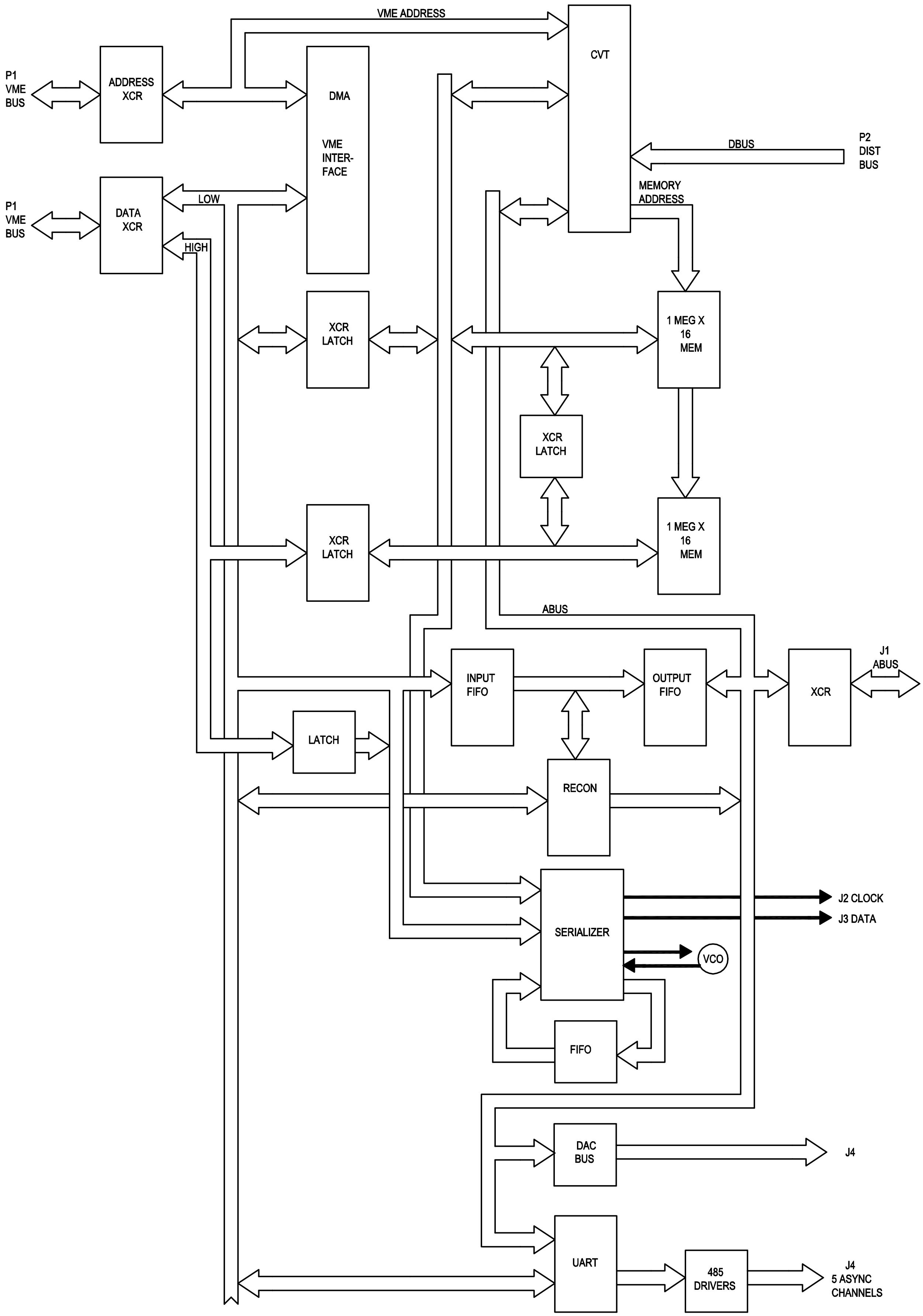
MODE	1	2	3
DELAY	460-520nS	700-760nS	940-1000nS

DIAG. 7000192 REV. A

SECTION 4
THEORY OF OPERATION

4.1 BLOCK DIAGRAM

This section contains a block diagram of the SIMR cards.



6011512-50 SIMR BLOCK DIAGRAM

DIAG. 7000210 PG.1 REV A.

SECTION 5
ADJUSTABLE SWITCH & JUMPER SETTINGS

5.1 DESCRIPTION

The paragraphs below describe the selections available on the 512VE-50 SIMR card.

5.1.1 U12, U13 - Address Select

U12 and U13 select the base of the 64 byte block of SIMR registers in the A16:D16 address space A6 through A15. U13 switches 1-8 select the eight MSBs and U18 switches 1-2 select the two LSBs. Switches 3-8 perform other functions described below. The card is factory set to address 65CX as shown in Figure 5-1.

5.1.2 U12 - Miscellaneous

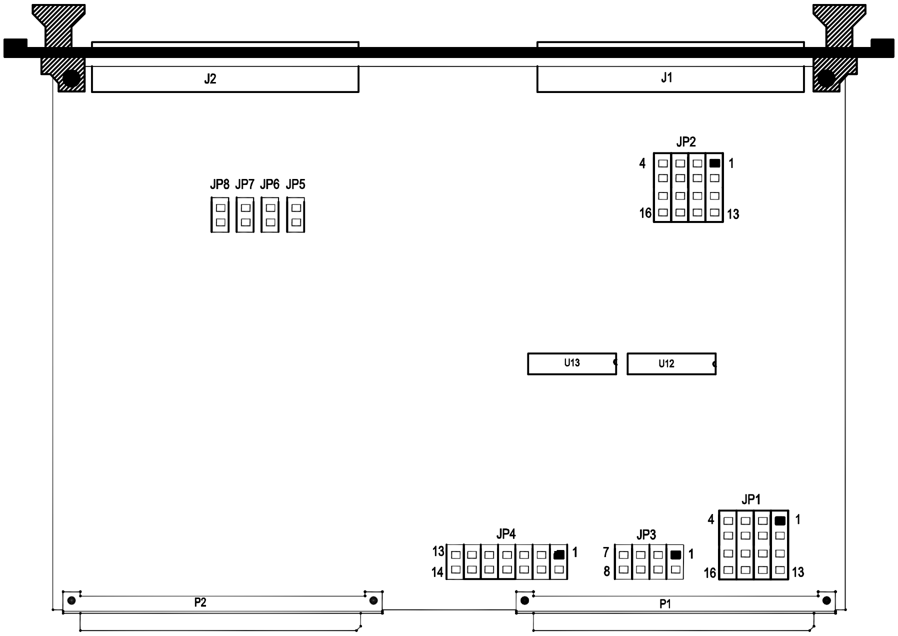
U12 switches 3, 4, & 5 select the Interrupt Acknowledge level. The switches are coded in binary with switch 3 the MSB, switch 5 the LSB. These switches must be set to the same interrupt level as the Interrupt Request level (JP4) selection.

SWITCH U12			DISPLAY
3	**4**	**5**	**Description**
On	On	On	Interrupt level 7
On	On	Off	Interrupt level 6
On	Off	On	Interrupt level 5
On	Off	Off	Interrupt level 4
Off	On	On	Interrupt level 3
Off	On	Off	Interrupt level 2
Off	Off	On	Interrupt level 1
Off	Off	Off	Invalid interrupt level

Switch 6 of U12 selects the address mode for the DMA transfers. Switch 6 ON selects A32 mode; OFF selects A24 mode. Switches 7 & 8 indicate the presence or absence of options on the SIMR card. The switches control bits 12 & 13 in the signature register, used for software configuration control. Switch 7 is set OFF when the *reconstructor* is installed. Bit 8 is set OFF when the *serializer* is installed.

5.1.3 A-bus Level Selection

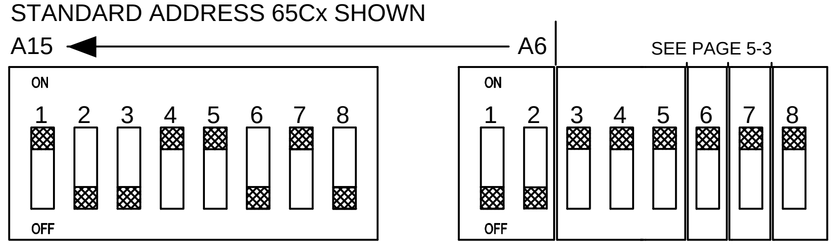
The reconstructor is a source of data on the A-bus and must have a Request and Grant level. These are assigned via JP2 selections. The 504VA DIST card and the 505V PDSP card are also bus masters. This means that the switch settings on the SIMR depend upon the system configuration.



STANDARD ADDRESS 65Cx SHOWN

ON = 0

OFF = 1



U13

ON								
OFF								

U12

ON								
OFF								

SHIPPED ADDRESS ____________________

CARD 6011512-50

SERIAL# / REV. ____________________

____
CUSTOMER JOB#

____
CONFIGURED BY DATE

____
QC CHECK BY DATE

JP5

IN	
OUT	

JP6

IN	
OUT	

JP7

IN	
OUT	

JP8

IN	
OUT	

JP3

PINS	INSTALLED
1-2	
3-4	
5-6	
7-8	

JP4

PINS	INSTALLED
1-2	
3-4	
5-6	
7-8	
9-10	
11-12	
13-14	

JP1

PINS	INSTALLED
1-5	
2-6	
3-7	
4-8	
9-13	
10-14	
11-15	
12-16	
5-9	
6-10	
7-11	
8-12	

JP2

PINS	INSTALLED
1-5	
2-6	
3-7	
4-8	
9-13	
10-14	
11-15	
12-16	

FIGURE 5-1. 512VE (SIMR) FACTORY SETTINGS

JP2 - A BUS SELECT

PINS	FUNCTION
1-5	A-BUS OUTPUT REQUEST 0
2-6	A-BUS OUTPUT REQUEST 1
3-7	A-BUS OUTPUT REQUEST 2
4-8	A-BUS OUTPUT REQUEST 3
9-13	A-BUS OUTPUT ACKNOWLEDGE 0
10-14	A-BUS OUTPUT ACKNOWLEDGE 1
11-15	A-BUS OUTPUT ACKNOWLEDGE 2
12-16	A-BUS OUTPUT ACKNOWLEDGE 3
REQUEST & ACKNOWLEDGE MUST MATCH	

JP1 - VME BUS GRANTS

PINS	FUNCTION
1-5	BUS GRANT IN 0 SELECT
2-6	BUS GRANT IN 1 SELECT
3-7	BUS GRANT IN 2 SELECT
4-8	BUS GRANT IN 3 SELECT
9-13	BUS GRANT OUT 0 SELECT
10-14	BUS GRANT OUT 1 SELECT
11-15	BUS GRANT OUT 2 SELECT
12-16	BUS GRANT OUT 3 SELECT
5-9	BYPASS BG IN O TO BG OUT 0
6-10	BYPASS BG IN 1 TO BG OUT 1
7-11	BYPASS BG IN 2 TO BG OUT 2
8-12	BYPASS BG IN 3 TO BG OUT 3
THE THREE UNSELECTED BUS GRANTS MUST BE BYPASSES	

JP4 - VME INTERRUPT REQUEST

PINS	FUNCTION
1-2	INTERRUPT REQUEST 1 SELECT
3-4	INTERRUPT REQUEST 2 SELECT
5-6	INTERRUPT REQUEST 3 SELECT
7-8	INTERRUPT REQUEST 4 SELECT
9-10	INTERRUPT REQUEST 5 SELECT
11-12	INTERRUPT REQUEST 6 SELECT
13-14	INTERRUPT REQUEST 7 SELECT

NOTE: INTERRUPT LEVEL ON JP4 MUST MATCH LEVEL SELECTED ON U19

JP3 - VME BUS REQUEST

PINS	FUNCTION
1-2	BUS REQUEST 0 SELECT
3-4	BUS REQUEST 1 SELECT
5-6	BUS REQUEST 2 SELECT
7-8	BUS REQUEST 3 SELECT

NOTE: BUS REQUEST, BUS GRANT IN, AND BUS GRANT OUT MUST MATCH

U12 - MISCELLANEOUS

SW	BIT	FUNCTION
3	MSB	INTERRUPT
4	-	LEVEL SELECT (1-7)
5	LSB	OFF=0, ON=1
6	OFF	A24 DMA MODE
6	ON	A32 DMA MODE
7	OFF	RECONSTRUCTOR IN
7	ON	NO RECONSTRUCTOR
8	OFF	SERIALIZER IN
8	ON	NO SERIALIZER

CARD # 6011512-50

FIGURE 5-2. MODEL 512VE (SIMR) SELECTIONS

JP5,6 DAC BUS OPTIONS

JP5	JP6	FUNCTION
OUT	OUT	SLOW CYCLE MODE 3 *
IN	OUT	SLOW CYCLE MODE 2 *
OUT	IN	SLOW CYCLE MODE 1 *
IN	IN	FAST CYCLE (SEE FIG. 3-41)

* SEE TIMING DIAGRAM 3-40

J7 - FOR TEST ONLY

PINS	FUNCTION
IN	NORMAL OPERATION
OUT	TEST FUNCTION

J8 - FOR TEST ONLY

PINS	FUNCTION
IN	NORMAL OPERATION
OUT	TEST FUNCTION

CARD # 6011512-50

FIGURE 5-2. MODEL 512VE (SIMR) SELECTIONS

5.1.4 DMA Bus Grant & Request

JP1 selects the bus grant level for DMA transfers. The Bus Grant In, Bus Grand Out, and Bus Request (selected by JP3) must all be set to the same level. The Figure 5-1 example shows Bus Grant In and Bus Grant Out set to level 2, and bypass connections are in for bus levels 0, 1, & 3. The Bus Request level (JP3) is also set for level 2. JP1 also selects Bus Grant Passthrough; the three bus levels that are not used by the DMA must be selected in the Bypass position.

5.1.5 Interrupt Request Level Select

JP4 selects the Interrupt Request level. The Interrupt Acknowledge level is selected with switches 3-5 of U12. The Interrupt Request and Acknowledge levels must be set to the same level.

5.1.6 DAC Bus Options

JP5 and JP6 select the Slow or Fast Cycle Modes. See Figures 3-40 and 3-41 for timing diagrams.

SECTION 6
DRAWINGS

6.1 INTRODUCTION TO THE DRAWINGS

Section 6 contains a complete technical drawing package describing your VME card. the drawings in this section are keyed to your specific serial numbered card.

6.1.1 Drawing System

Acroamatics Drawing numbers are seven digit numbers which can also have a two digit dash number. The first four digits represent a drawing class, and wherever a drawing may be part of a standard drawing package, drawing numbers are issued so that all drawings which are part of the package share the same last three digits. In the following discussion “xxx” represents the number keyed to the the card part number (6011xxx). Individual parts are classified within the same drawing system, but are assigned serially without regard to other assemblies.

The PC Card Reference package includes the following drawings:

FOR CARD PART NUMBER 60115xx:

60115xx	Card Assembly Drawing
81115xx	Card List of Materials
21115xx	Card Schematic Drawing

6.1.2 Drawing Package Organization

This section of the manual contains the physical drawings, called *Drawings*, as opposed to the schematic drawings, called *Schematics*, which are found in Section 7.

The Drawings section includes the card component assembly drawing 60115nn and the card List Of Materials (LOM). LOM’s include sufficient information to facilitate ordering replacement parts either from Acroamatics or from the original component manufacturer. LOMs list parts by Acroamatics Part Number in the column headed *PART NO* . The component manufacturer is identified as *VENDOR*. Parts for which ACROAMATICS is listed as vendor are proprietary components available only from Acroamatics, Inc. Integrated Circuits which are industry standard are listed as GENERIC, and may be obtained from any reliable vendor. Other parts for which a specific source is listed may be available from other sources. When substituting parts from vendors other than those specifically listed, be certain that the components are truly interchangeable.

The last column (Reference) of the List of Materials lists the assembly location or locations. An assembly location can contain a socket as well as the component plugged into the socket.

For example

U15

S1

74ALS244

This example shows that location U15 contains socket S1 and an IC of type 74ALS244. Resistors, capacitors, and other components are shown in a similar fashion, and are referenced using common industry abbreviations.

6.1.3 Programmed Parts

The VME card can include programmed parts such as PROMs, EPROMs, EEPROMs, PALs, GALs, FPGAs, etc. If these are a permanent part of the hardware, they are documented on the List Of Materials for the PC card on which they are installed. Programmed parts are listed on the LOM twice; once as the unprogrammed part, with the Manufacturers Part Number, and also under the Acroamatics program number (606xxxx) with which they must be programmed to become the correct programmed part.

Programs for PROMs have part numbers in the series 6061xxx
Programs for EPROMs and EEPROMs have part numbers in the series 6062xxx
Programs for PALws and GALs have part numbers in the series 6064xxx
Programs for FPGAs have part numbers in the series 6067xxx

REV	REASON	MANDATORY	INITIATED BY	APPRV	DATE
A	RELEASED SEE ECR #4639		HC		9/00
B	SEE ECR #4670		BL		10/00
C	SEE ECR #4727		HC		4/01
D	SEE ECR #4771		B.L.		1/02
E	SEE ECR #4985		B.L.		9/04

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X	X	X	X																					

LIST OF MATERIALS 8111512-50

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X																									

PC CARD 1290226

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X	X	X																						

SCHEMATICS 2111512-50

MANUFACTURING:

VERIFY REVISION LEVELS OF WIRELIST AND L.O.M. BEFORE BUILDING CARD.

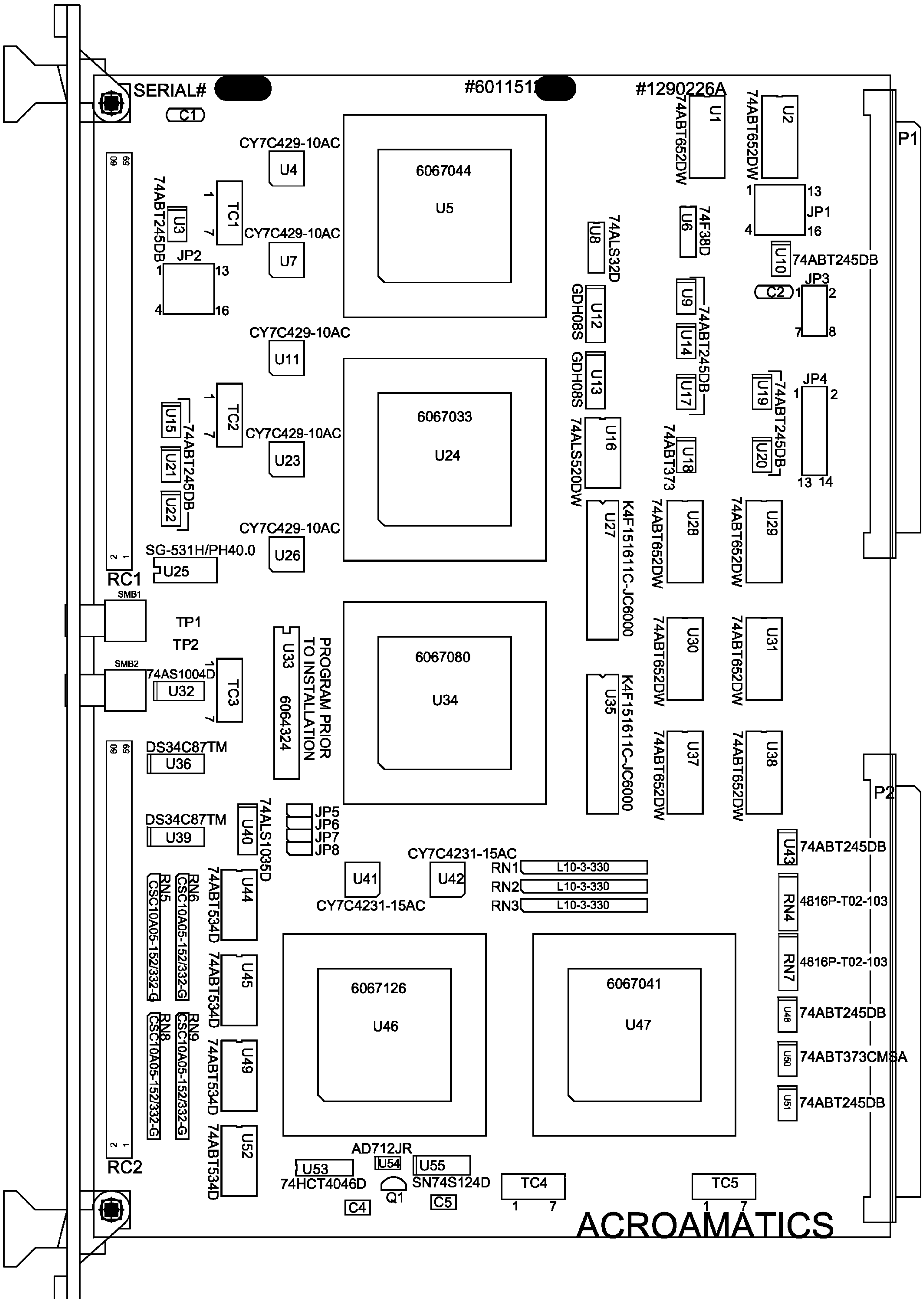
DR	D MACDONALD	9/04
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

VME SIMR SIM/REC/ASYN/DAC BUS

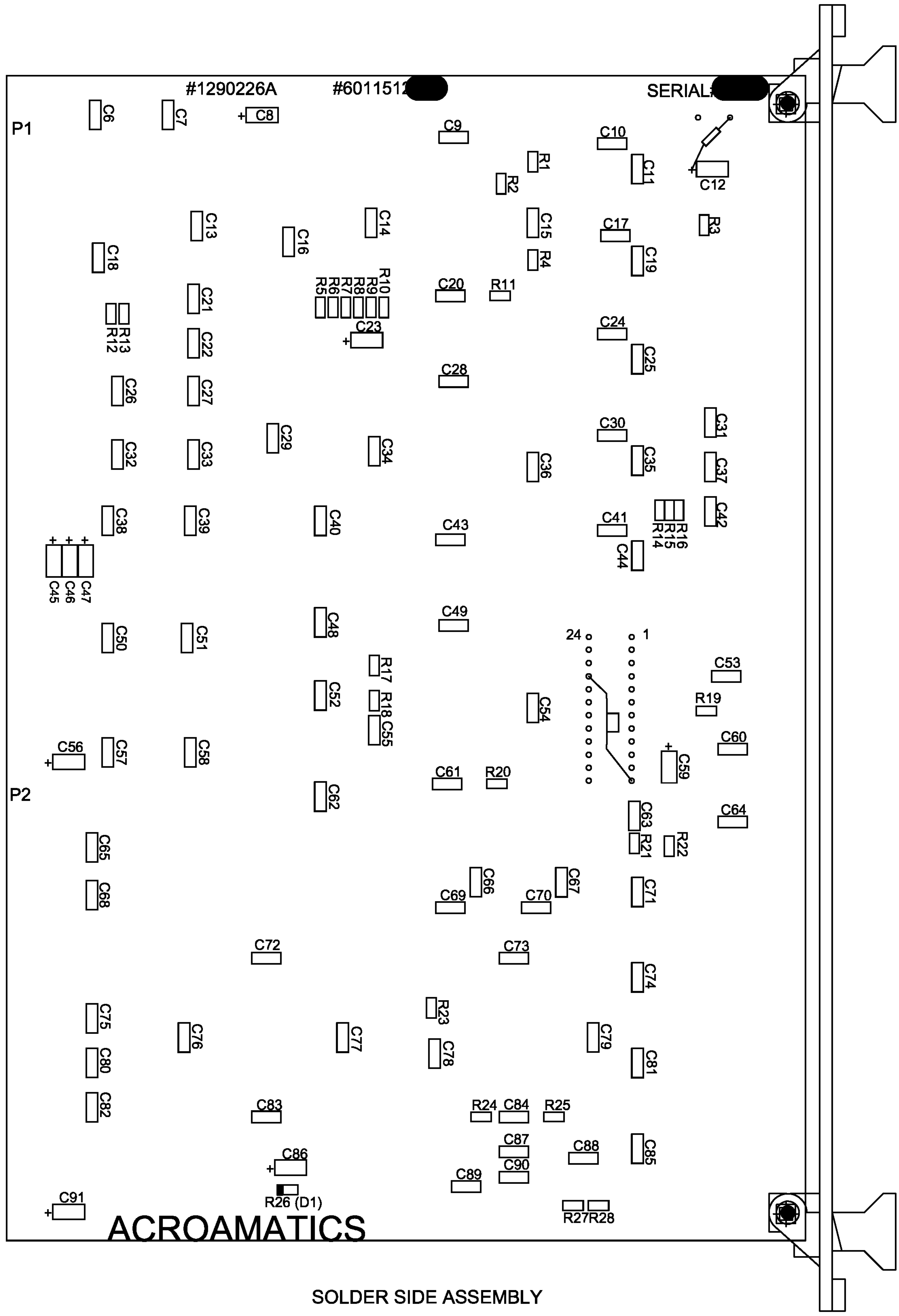
SIZE	SCALE	DWG NO.
B	NTS	6011512-50
SHEET	1 OF 3	REV E



VIEW AS SEEN FROM COMPONENT SIDE

IMPORTANT : ALL ACTELS MUST BE PROGRAMMED BEFORE SOLDERING

DR	D MACDONALD	9/04	ACROAMATICS TELEMETRY SYSTEMS GOLETA, CAL. 93117	
CHK				
APPD			ASSEMBLY, CIRCUIT CARD	
			VME SIMR SIM/REC/ASYN/DAC BUS	
NEXT ASSY	USED ON		SIZE B	SCALE NTS	DWG NO. 6011512-50
APPLICATION			SHEET 2 OF 3	REV E



SOLDER SIDE ASSEMBLY

1. Solder capacitor PN 1902161 from pin 21 to pin 12 of U33
2. Solder a resistor PN 7685002 from C12+ to old solder pad C1 closest to front panel

DR	D MACDONALD	9/04	ACROAMATICS TELEMETRY SYSTEMS GOLETA, CAL. 93117
CHK			
APPD			ASSEMBLY, CIRCUIT CARD
			VME SIMR SIM/REC/ASYN/DAC BUS
NEXT ASSY	USED ON		SIZE B · SCALE NTS · DWG NO. 6011512-50
APPLICATION			SHEET 3 OF 3 · REV E

LIST OF MATERIALS 8111512-50 PAGE 1 OF 2
VME SIMR SIM/REC/ASYN/DAC B

ASSEMBLY PN 6011512-50 DRAWN BY Howard Sep 10 14:47

REVISION E ENGINEERING APPROVAL _______________ DATE ________

MANUFACTURING APPROVAL _______________ DATE ________

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
1	1290226	1	PCB VME SIMR (-50)	1290226	ACROAMATICS	
2						
3	1902161	2	CAP CERM 100pF 50V	CN15C101J	CENTRALAB	C1,C2
4						
5	1903002	1	CAP TMP STBL (X7R) 0.12uF	C320C124K5R5CA	KEMET	C4
6	1871056	1	CAP SILV MICA 3pF 50V	CD5CC030D03	CD	C5
7	1902172	76	CAP CERM .1uF 50V X7R SMT	C1206C104K5RAC	KEMET	C6,C7,C9,C10,C11,C13,C14,C15,C16
7						C17,C18,C19,C20,C21,C22,C24,C25,
7						C26,C27,C28,C29,C30,C31,C32,C33,
7						C34,C35,C36,C37,C38,C39,C40,C41
7						C42,C43,C44,C48,C49,C50,C51,C52,
7						C53,C54,C55,C57,C58,C60,C61,C62,
7						C63,C64,C65,C66,C67,C68,C69,C70
7						C71,C72,C73,C74,C75,C76,C77,C78,
7						C79,C80,C81,C82,C83,C84,C85,C87,
7						C88,C89,C90
8	1922656	10	CAP TA 10uF 10% 20V SMT	T491B106K020AS	KEMET	C8,C12,C23,C45,C46,C47,C56,C59,
8			Acceptable substitute is:	ECS-T1DX106R	PANASONIC	
8						C86,C91
9						
10	2796061	2	CONN PC 96P SDR RTANGL	7296-50C2TH	3M	P1.P2
11	2796059	2	CONN PC 60P SDR RTANGL	2560-5002UB	3M	RC1,RC2
12	2796057	2	CONN PC SMB RTANGLE 1P	903-373J-51A	AMPHENOL	SMB1,SMB2
13	2796104	5	CONN PC 7PIN 1.25 HEADER SMT	53398-0790	MOLEX	TC1,TC2,TC3,TC4,TC5
14						
15	7580019	1	REGULATOR +5V 100mA 5%	MC78L05ACP	MOTOROLA	Q1
15			Acceptable substitute is:	LM78L05ACZ	NATIONAL	
16	7700047	3	RES SIP 33 OHM 5R 10P	L10-3-330	BECKMAN	RN1,RN2,RN3
17	7700036	4	RES SIP 1.5K/3.3K 10P 2%	CSC10A05-152/332-G	DALE	RN5,RN6,RN8,RN9
18	7690103	2	RES DIP 10K OHM 15R 16P SMT	4816P-T02-103	BOURNS	RN7,RN4
19	7680981	19	RES 10K .1W 1% SMT-0805	ERJ-6ENF10.0K	PANASONIC	R1,R4,R5,R6,R7,R8,R9,R10,R11,R13,
19						R14,R15,R16,R20,R23,R24,R25,R27,
19						R28
20	7680979	6	RES 1K .1W 1% SMT-0805	ERJ-6ENF1.00K	PANASONIC	R2,R3,R17,R18,R21,R22
21	7680932	1	RES 46.4 OHM .1W 1% SMT-0805	ERJ-6ENF46.4	PANASONIC	R12
22	7680984	1	RES 200 OHM .1W 1% SMT-0805	ERJ-6ENF200	PANASONIC	R19
23	7685002	1	RESISTOR 1K 1/8W 1%	5063JD1K00F	PHILIPS	R29
24	3573821	1	DIODE SCHOTTKY SMT 200mA	MA2SD10CT-ND	PANASONIC	(D1) IN LOCATION R26
25						
26	6350042	1	OSCIL. XTAL 40MHz DIP	SG-531H/PH-40.00	EPSON	U25
27						
28	5300652-49	8	IC OCT BUS/REG XCVR NI TS SMT	74ABT652-DW	GENERIC	U1,U2,U28,U29,U30,U31,U37,U38
28			Acceptable substitute is:	74ABT652-ADW	GENERIC	
29	5300245-91	13	IC OCT BUS XCVR NI TS SMT	74ABT245DB	GENERIC	U3,U9,U10,U14,U15,U17,U19,U20,U21,
29						U22,U43,U48,U51

VME SIMR SIM/REC/ASYN/DAC B

ASSEMBLY PN 6011512-50 DRAWN BY Howard Sep 10 14:47

REVISION E

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
30	5308429-10	5	IC 2Kx9-BIT FIFO (QFP)	CY7C429-10AC	CYPRESS	U4,U7,U11,U23,U26
31	5300038-39	1	IC QUAD 2-INP NAND BUFF(SMD)	N74F38D	GENERIC	U6
32	5300032-39	1	IC QUAD 2-INP OR GATE SMT	74ALS32D	GENERIC	U8
33	5300520-32	1	IC 8-BIT MAG COMP SMT	74ALS520DW	GENERIC	U16
34	5300373-91	2	IC OCT D-LATCH TRANSP TS SMT	SN74ABT373ADB	TI	U50,U18
34			Acceptable substitute is:	74ABT373CMSA	NATIONAL	
35	5336967-02	2	IC 1Mx16 CMOS DRAM 60ns SOJ	K4F151611C-JC6000	SAMSUNG	U27,U35
35			Acceptable substitute is:	KM16C1200CJ-6	SAMSUNG	
36	5302034	1	IC HEX INVERTER (SMD)	74AS1004D	TI	U32
37	5308487-02	2	IC QUAD DIFF XMTR SOP	DS34C87TM	NATIONAL	U39,U36
38	5300035-32	1	HEX OPEN COLLECTOR BUFFER SMT	74ALS1035D	TI	U40
39	5308423-15	2	IC 2Kx9 SYNCHRONOUS FIFO SMT	CY7C4231-15AC	CYPRESS	U42,U41
39			Acceptable substitute is:	IDT72231L15PF	IDT	
40	5300534-49	4	IC OCTAL D-LATCH, INVERTED SMT	74ABT534D	SIGNETICS	U44,U45,U49,U52
41	5301046-51	1	IC PLL/VCO CMOS,SMT	74HCT4046D	RCA/SIG	U53
42	5301712	1	IC OP AMP DUAL PRECISION SMT	AD712JR	ANALOG-DEVICES	U54
43	5300124-07	1	IC DUAL VLTG-CONTROLLED OSC.	SN74S124D	TI	U55
44						
45	5353017	1	IC GAL 22V10 10ns 24P	GAL22V10B-10LP	LATTICE	unprogrammed GAL
46	5354009	1	FPGA 8000 GATE QFP	A1280XL-PQ160C	ACTEL	unprogrammed FPGA
47	5354010	4	FPGA 4000 GATE QFP	A1240XL-PQ144C	ACTEL	unprogrammed FPGA
48						
49						
50	6067044	1	VME SIMR DMA CTL	5354010-REV.D	ACROAMATICS	U5,RECVME2,Item 47
51	6067033	1	VME SIMR RECONSTRUCTOR	5354010-REV.D	ACROAMATICS	U24,REC,Item 47
52	6064324	1	VME SIMR OUTPUT BUS CNTRLER	5353017-REV.B	ACROAMATICS	PROGRAM PRIOR TO INSTALLATION
52						U33,Item 45
53	6067080	1	VME SIMR 5 SYNC/DAC BUS	5354010-REV.B	ACROAMATICS	U34,SIMR7080,Item 47
54	6067126	1	VME SIMR (-50) SERIAL MODE B	5354010-REV.A	ACROAMATICS	U46,SIMR7126,Item 47
55	6067041	1	VME SIMR FORMATTER	5354009-REV.D	ACROAMATICS	U47,FRMBUF,Item 46
56						
57	9070015	2	DIP SWITCH 8-POS SLIDE SMT	GDH08S	AUGAT	U13,U12
58	5470011	1	JUMPER PINS SINGLE ROW 50POS	MTSW-150-07-G-S-24	SAMTEC	TP1,TP2
59	5470012	2	JUMPER PINS DOUBLE ROW 50POS	MTSW-150-07-G-D-24	SAMTEC	JP2(4X4),JP1(4X4),JP3(2X4)
59						JP4(2X7),JP5-JP8(1X2)
60	5600012	1	LABEL,VME PNL, ACRO	5600012	ACROAMATICS	
61	5600022	1	LABEL,VME PNL, SIMR	5600022	ACROAMATICS	
62	6730092	1	FR PNL-VME BLANK	6U4EF0000	TRIPLE-E	SCRN #8071150, MOD #5951095