

DN 6000277

TECHNICAL MANUAL
MODEL 514V

• QUAD PARALLEL OUTPUT INTERFACE •

Acroamatics, Inc.

70 South Kellogg Avenue
Goleta, CA 93117-3476

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ACROAMATICS DOCUMENT HISTORY

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SECTION 1
INTRODUCTION

1.1 DESCRIPTION

The Model 514V QPOI card is a VME-compatible 6U card that provides up to four output channels from the *Device Bus (A-Bus)* to any of the following: an external host computer such as the Acroamatics Model 5110 System Control Unit (SCU), a DEC computer equipped with a DR11W or DRV11W interface, a Gould Instruments TA4000 series strip chart recorder equipped with a digital input interface, or a 32-bit parallel output interface to a digital processing unit such as the Acroamatics Model 2420 Digital to Analog Converter. QPOI input is over the Device Bus, which provides processed and formatted telemetry data that you can programmably direct to any of the eight output devices that use this bus. Data processing occurs in the 504VA DIST and 505V PDSP cards. The telemetry compiler provides the software path that allows you to select the programmable message processing and output distribution on the device bus for a specific application.

1.2 DR11W & DRV11W INTERFACE

The 514V card can include circuitry supporting data transfers from the Acroamatics Telemetry Data Processor to a DEC computer equipped with a DR11W or DRV11W interface card. The device bus device number is switch-selectable to support multi-channel configurations. The 16-bit output channels are not available when this option is selected.

1.3 32 BIT PARALLEL OUTPUT

You can configure this channel to be compatible with the DAC Bus, which is the input to external DAC circuits housed in our Model 2420 series chassis, or as a general purpose output channel. The output provides 16 data and 16 address lines along with an output strobe. The Device Bus device number is switch selectable, but is set to Device 7 to simulate the DAC bus function. You can use other device settings for general purpose data interfacing, and select the output format as 32-bit data or 16-bit data with ID tags.

1.4 16 BIT OUTPUT CHANNELS

The 514V card also provides three 16 bit host computer interface channels for outputting processed data from the device bus. Output channel A is equipped with a *Request* and a *Grant* signal so that you can transfer your data via an external DMA channel. Output channel B provides 16 data lines with control signals to transfer data to two separate input ports. You can program-select the data to go to *Channel 1*, *Channel 2*, or *Both*. Both channels A & B have a switch-selectable *device address* and are configured to allow multi-channel data input structures. The DR11 interface is not available when this option is selected.

1.5 STRIP CHART FORMATTING

Output channel C receives data from either the A-Bus or the VMEBus as 32 bit messages, then formats the data for transfer to a TA4000 series thermal digital strip chart recorder as two 16 bit transfers. This channel processes messages to Device 7.

1.6 OPTIONS

The following options are available with the 514V.

514V-01	16-bit SCU I/F & 32-bit DAC bus.
514V-02	16-bit SCU I/F, Digital TA4000 I/F, & 32-bit DAC bus.
514V-03	DR-11 I/F, Digital TA4000 I/F, & 32-bit DAC bus.
514V-04	DR-11 I/F & 32-bit DAC bus.

1.7 DOCUMENT CONVENTIONS

In this document register addresses and address offsets are hexadecimal numbers. Where it is necessary to refer to a hexadecimal number in the text, we use the C programming convention *0xNN* to refer to hexadecimal number *NN*. Bits in a register are numbered in decimal. The term *Device n* refers to an address destination on the TDP system A-Bus. The A-bus is the output data bus, and has eight possible destination devices. Although we do not use all eight, those destinations we do use are dedicated to specific functions in the TDP system. The term *DIT* refers to a data message in the TDP system. It stands for "Data, ID, and Time", the three components of a TDP data message. We can label a DIT by the value of its ID tag, for example "DIT 0xFFF1", the DIT that conveys the once per millisecond value of a time message. Frequently we use a functional label instead, for example, "the MILLISECOND DIT".

SECTION 2 INSTALLATION

2.1 GENERAL

This section contains installation information for the Acroamatics Model 514V Quad Parallel Output Interface (QPOI). The card part number is 6011514.

2.2 UNPACKING

Using proper ESD-protection procedures, open the cardboard shipping container and remove the card from the anti-static bag. Retain the container, anti-static bag, and foam packaging material for use if you must return the card.

2.3 FACTORY RETURN

When you return a card to the factory for repair or modification, include as much information as possible describing the failure mode or the modification~update you want.

Pack the card for shipment by wrapping it in the anti-static bag. Place the card into the shipping container, protecting it with the foam packing, and secure the container with reinforced tape. Provide the name and phone number of a technical contact we can talk to regarding the card.

Call Acroamatics at (805) 967-9909 to get an RMA number before returning any equipment to the factory, and include the RMA number in any correspondence or shipments to Acroamatics.

2.4 INSTALLING

The QPOI card mounts in a standard VMEbus chassis. Mounting dimensions are shown in the assembly Drawing in Section 6 of this manual. Slide the card into one of your system VME chassis slots and seat the card firmly by pressing against the ears. Make the front panel cable connections appropriate to your system. Remove the board by pulling firmly on the outside of the ears.

2.5 CONNECTORS

The following pages contain tables of information on all the connections into and out of the QPOI card.

TABLE 2-1. MATING CONNECTOR LIST FOR MODEL 514V VERSIONS 514V-01, 514V-02, 514V-03, 514V-04		
CONN.	FUNCTION	MATING CONNECTOR
P01	VMEbus	603-2-IEC-C096F
P02	VMEbus, Digital Port 1, & Remote Device Setup/Verify	603-2-IEC-C096F
J01	OUTPUT DEVICE BUS	3334-6660 (3M)
J02	Channel B Output Bus (-01, -02)	3417-6640 (3M)
J02	DR11 Input Bus (-03, -04)	3417-6640 (3M)
J03	Channel A Output Bus (-01, -02)	3417-6640 (3M)
J03	DR11 Output Bus (-03, -04)	3417-6640 (3M)

TABLE 2-2. CONNECTOR LIST		
MODEL 514V BACKPLANE CONNECTOR P01-ROW-A		
NOTE: ALL (\$) SIGNALS UNUSED ON THIS CARD		
PIN	SIGNAL	FUNCTION
01	4VMED00	Data Bus 00
02	4VMED01	Data Bus 01
03	4VMED02	Data Bus 02
04	4VMED03	Data Bus 03
05	4VMED04	Data Bus 04
06	4VMED05	Data Bus 05
07	4VMED06	Data Bus 06
08	4VMED07	Data Bus 07
09	GND	Ground
10	SYCLK	System Clock
11	GND	Ground
12	9VMEDS1	Data Strobe 1
13	9VMEDS0	Data Strobe 0
14	9VMEWRT	Write
15	GND	Ground
16	9VMDACK	Data Transfer Acknowledge
17	GND	Ground
18	9VMASTB \$	Address Strobe
19	GND	Ground
20	9VMIACK	Interrupt Acknowledge
21	9VMIAIN \$	Interrupt Acknowledge IN
22	9VMIAOT \$	Interrupt Acknowledge OUT
23	4VMAM04	Address Modifier 4
24	4VMEA07	Address Bus 07
25	4VMEA06	Address Bus 06
26	4VMEA05	Address Bus 05
27	4VMEA04	Address Bus 04
28	4VMEA03	Address Bus 03
29	4VMEA02	Address Bus 02
30	4VMEA01	Address Bus 01
31	-12 VDC \$	-12 Volts DC
32	+5 VDC	+5 Volts DC

**TABLE 2-3. CONNECTOR LIST
MODEL 514V BACKPLANE CONNECTOR P01-ROW-B**

NOTE: ALL (\$) SIGNALS UNUSED ON THIS CARD		
PIN	SIGNAL	FUNCTION
01	9VMSBY \$	Bus Busy
02	9VMBCLR \$	Bus Clear
03	ACFAIL \$	AC Power Fail
04	9VMBGI0 \$	Bus Grant 0 IN
05	9VMBGO0 \$	Bus Grant 0 OUT
06	9VMBGI1 \$	Bus Grant 1 IN
07	9VMBGO1 \$	Bus Grant 1 OUT
08	9VMBGI2 \$	Bus Grant 2 IN
09	9VMBGO2 \$	Bus Grant 2 OUT
10	9VMBGI3 \$	Bus Grant 3 IN
11	9VMBGO3 \$	Bus Grant 3 OUT
12	9VMBRQ0 \$	Bus Request 0
13	9VMBRQ1 \$	Bus Request 1
14	9VMBRQ2 \$	Bus Request 2
15	9VMBRQ3 \$	Bus Request 3
16	4VMAM00	Address Modifier 0
17	4VMAM01	Address Modifier 1
18	4VMAM02 \$	Address Modifier 2
19	4VMAM03	Address Modifier 3
20	GND	Ground
21	SERCLK \$	Serial Clock
22	SERDAT \$	Serial Data
23	GND	Ground
24	9VMIRQ7 \$	Interrupt Request 7
25	9VMIRQ6 \$	Interrupt Request 6
26	9VMIRQ5 \$	Interrupt Request 5
27	9VMIRQ4 \$	Interrupt Request 4
28	9VMIRQ3 \$	Interrupt Request 3
29	9VMIRQ2 \$	Interrupt Request 2
30	9VMIRQ1 \$	Interrupt Request 1
31	+5 VSTDBY \$	Stand-by +5 Volts DC
32	+5 VDC	+5 Volts DC

TABLE 2-4. CONNECTOR LIST		
MODEL 514V BACKPLANE CONNECTOR P01-ROW-C		
NOTE: ALL (\$) SIGNALS UNUSED ON THIS CARD		
PIN	SIGNAL	FUNCTION
01	4VMED08	Data Bus 08
02	4VMED09	Data Bus 09
03	4VMED10	Data Bus 10
04	4VMED11	Data Bus 11
05	4VMED12	Data Bus 12
06	4VMED13	Data Bus 13
07	4VMED14	Data Bus 14
08	4VMED15	Data Bus 15
09	GND	Ground
10	SYSFAIL \$	System Failure
11	9VMBERR \$	Bus Error
12	9VMPRST	System Reset
13	9VMELWD	Long Word
14	4VMAM05	Address Modifier 5
15	4VMEA23 \$	Address Bus 23
16	4VMEA22 \$	Address Bus 22
17	4VMEA21 \$	Address Bus 21
18	4VMEA20 \$	Address Bus 20
19	4VMEA19 \$	Address Bus 19
20	4VMEA18 \$	Address Bus 18
21	4VMEA17 \$	Address Bus 17
22	4VMEA16 \$	Address Bus 16
23	4VMEA15	Address Bus 15
24	4VMEA14	Address Bus 14
25	4VMEA13	Address Bus 13
26	4VMEA12	Address Bus 12
27	4VMEA11	Address Bus 11
28	4VMEA10	Address Bus 10
29	4VMEA09	Address Bus 09
30	4VMEA08	Address Bus 08
31	+12 VDC \$	+12 Volts DC
32	+5 VDC	+5 Volts DC

PIN	SIGNAL	FUNCTION
01	DADB00 -	DAC Data Bus 00 - LSB
02	DADB02 -	DAC Data Bus 02
03	DADB04 -	DAC Data Bus 04
04	DADB06 -	DAC Data Bus 06
05	DADB08 -	DAC Data Bus 08
06	DADB10 -	DAC Data Bus 10
07	DADB12 -	DAC Data Bus 12
08	DADB14 -	DAC Data Bus 14
09	Ground	
10	DAAB01 -	DAC Address Bus 01
11	DAAB03 -	DAC Address Bus 03
12	DAAB05 -	DAC Address Bus 05
13	DAAB07 -	DAC Address Bus 07
14	DAAB09 -	DAC Address Bus 09
15	DAAB11 -	DAC Address Bus 11
16	DAAB14 -	DAC Address Bus 14
17	DAAB00 -	DAC Address Bus 00 - LSB
18	DACWAT -	Bus Wait
19	NC	
20	NC	
21	CHRT01 +	Chart Recorder Data Bus 01
22	Ground	
23	CHRT04 +	Chart Recorder Data Bus 04
24	Ground	
25	CHRT07 +	Chart Recorder Data Bus 07
26	Ground	
27	CHRT10 +	Chart Recorder Data Bus 10
28	Ground	
29	CHRT13 +	Chart Recorder Data Bus 13
30	CHRT15 +	Chart Recorder Data Bus 15 - MSB
31	Ground	
32	Ground	

TABLE 2-6. CONNECTOR LIST		
MODEL 514V BACKPLANE CONNECTOR P02-ROW-B		
NOTE: ALL (\$) SIGNALS UNUSED ON THIS CARD		
PIN	SIGNAL	FUNCTION
01	+5 VDC	+5 Volts DC
02	GND	Ground
03	RESERVED (\$)	
04	4VMEA24 (\$)	Address Bus 24
05	4VMEA25 (\$)	Address Bus 25
06	4VMEA26 (\$)	Address Bus 26
07	4VMEA27 (\$)	Address Bus 27
08	4VMEA28 (\$)	Address Bus 28
09	4VMEA29 (\$)	Address Bus 29
10	4VMEA30 (\$)	Address Bus 30
11	4VMEA31 (\$)	Address Bus 31
12	GND	Ground
13	+5 VDC	+5 Volts DC
14	4VMED16 (\$)	Data Bus 16
15	4VMED17 (\$)	Data Bus 17
16	4VMED18 (\$)	Data Bus 18
17	4VMED19 (\$)	Data Bus 19
18	4VMED20 (\$)	Data Bus 20
19	4VMED21 (\$)	Data Bus 21
20	4VMED22 (\$)	Data Bus 22
21	4VMED23 (\$)	Data Bus 23
22	GND	Ground
23	4VMED24 (\$)	Data Bus 24
24	4VMED25 (\$)	Data Bus 25
25	4VMED26 (\$)	Data Bus 26
26	4VMED27 (\$)	Data Bus 27
27	4VMED28 (\$)	Data Bus 28
28	4VMED29 (\$)	Data Bus 29
29	4VMED30 (\$)	Data Bus 30
30	4VMED31 (\$)	Data Bus 31
31	GND	Ground
32	+5 VDC	+5 Volts DC

**TABLE 2-7. CONNECTOR LIST
MODEL 514V BACKPLANE CONNECTOR P02-ROW-C**

NOTE: ALL (\$) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	DACAEB -	Address Cycle
02	DADB01 -	DAC Data Bus 01
03	DADB03 -	DAC Data Bus 03
04	DADB05 -	DAC Data Bus 05
05	DADB07 -	DAC Data Bus 07
06	DADB09 -	DAC Data Bus 09
07	DADB11 -	DAC Data Bus 11
08	DADB13 -	DAC Data Bus 13
09	DADB15 -	DAC Data Bus 15 - MSB
10	DACSTB -	DAC Strobe
11	DAAB02 -	DAC Address Bus 02
12	DAAB04 -	DAC Address Bus 04
13	DAAB06 -	DAC Address Bus 06
14	DAAB08 -	DAC Address Bus 08
15	DAAB10 -	DAC Address Bus 10
16	DAAB12 -	DAC Address Bus 12
17	DAAB15 -	DAC Address Bus 15 - MSB
18	Ground -	
19	DAAB13 -	DAC Address Bus 13
20	NC	
21	CHRT00 +	Chart Recorder Data Bus 00 - LSB
22	CHRT02 +	Chart Recorder Data Bus 02
23	CHRT03 +	Chart Recorder Data Bus 03
24	Ground	
25	CHRT06 +	Chart Recorder Data Bus 06
26	CHRT08 +	Chart Recorder Data Bus 08
27	CHRT09 +	Chart Recorder Data Bus 09
28	CHRT11 +	Chart Recorder Data Bus 11
29	CHRT12 +	Chart Recorder Data Bus 12
30	CHRT14 +	Chart Recorder Data Bus 14
31	TABUSY -	Chart Recorder Busy
32	TASTRB -	Chart Recorder Strobe

TABLE 2-8. CONNECTOR LIST
MODEL 514V FRONT PANEL CONNECTOR J01

PIN	SIGNAL	FUNCTION
01		Not Used
02	9AWORD1	A Bus Last Word Flag
03	4SFLAG1	A Bus Last Transfer Flag
04	4APORT1	A Bus Port Select 1
05	GND	Ground
06	4APORT0	A Bus Port Select 0
07	4ADEST2	A Bus Destination Select 2
08	4ADEST1	A Bus Destination Select 1
09	4ADEST0	A Bus Destination Select 0
10	4AOUT15	A Bus 15
11	4AOUT14	A Bus 14
12	GND	Ground
13	4AOUT13	A Bus 13
14	4AOUT12	A Bus 12
15	4AOUT11	A Bus 11
16	4AOUT10	A Bus 10
17	GND	Ground
18	4AOUT09	A Bus 09
19	4AOUT08	A Bus 08
20	4AOUT07	A Bus 07
21	4AOUT06	A Bus 06
22	4AOUT05	A Bus 05
23	4AOUT04	A Bus 04
24	GND	Ground
25	4AOUT03	A Bus 03
26	4AOUT02	A Bus 02
27	4AOUT01	A Bus 01
28	4AOUT00	A Bus 00
29	GND	Ground
30	9AOACK0	A Bus Acknowledge 0
31	9AOREQ0	A Bus Request 0
32	GND	Ground
33	9AOACK1	A Bus Acknowledge 1
34	9AOREQ1	A Bus Request 1
35	GND	Ground
36	9AOACK2	A Bus Acknowledge 2
37	9AOREQ2	A Bus Request 2
38	GND	Ground
39	9AOACK3	A Bus Acknowledge 3
40	9AOREQ3	A Bus Request 3

TABLE 2-8. (continued) CONNECTOR LIST MODEL 514V FRONT PANEL CONNECTOR J01		
NOTE: ALL (\$) SIGNALS UNUSED ON THIS CARD		
PIN	SIGNAL	FUNCTION
41	GND	Ground
42	9AOWAIT	A Bus Wait
43	9AOREST	A Bus Reset
44	GND (\$)	Ground
45		Not Used
46		↓
47		↓
48		↓
49		↓
50		↓
51		↓
52		↓
53		↓
54		↓
55		↓
56		↓
57		↓
58		Not Used
59	GND	Ground
60	9AOSTRB	A Bus Data Strobe

TABLE 2-9. CONNECTOR LIST		
FRONT PANEL CONNECTOR J02		
MODELS 514V-01 & 514V-02 ONLY		
PIN	SIGNAL	FUNCTION
01	4EDBB00	Channel B Output Bus 0
02	GND	Ground
03	4EDBB01	Channel B Output Bus 1
04	4EDBB02	Channel B Output Bus 2
05	GND	Ground
06	4EDBB03	Channel B Output Bus 3
07	4EDBB04	Channel B Output Bus 4
08	GND	Ground
09	4EDBB05	Channel B Output Bus 5
10	4EDBB06	Channel B Output Bus 6
11	GND	Ground
12	4EDBB07	Channel B Output Bus 7
13	4EDBB08	Channel B Output Bus 8
14	GND	Ground
15	4EDBB09	Channel B Output Bus 9
16	4EDBB010	Channel B Output Bus 10
17	GND	Ground
18	4EDBB011	Channel B Output Bus 11
19	GND	Ground
20	4EDBB012	Channel B Output Bus 12
21	GND	Ground
22	4EDBB013	Channel B Output Bus 13
23	GND	Ground
24	4EDBB014	Channel B Output Bus 14
25	GND	Ground
26	4EDBB015	Channel B Output Bus 15
27	GND	Ground
28	9EDBEOP	Last Word of Buffer
29	GND	Ground
30	4CH1DRY	Channel 1 Data Ready +
31	9CH1DRY	Channel 1 Data Ready -
32	4CH2DRY	Channel 2 Data Ready +
33	9CH2DRY	Channel 2 Data Ready -
34	4CH1RFD	Channel 1 Ready for Data +
35	9CH1RFD	Channel 1 Ready for Data -
36	4CH2RFD	Channel 2 Ready for Data +
37	9CH2RFD	Channel 2 Ready for Data -
38	GND	Ground
39		not used
40	GND	Ground

TABLE 2-10. CONNECTOR LIST		
FRONT PANEL CONNECTOR J02		
MODELS 514V-03 & 514V-04 ONLY		
PIN	SIGNAL	FUNCTION
01	4VODT15	DR11 Output Data Bus 15
02	4VODT00	DR11 Output Data Bus 0
03	4VODT14	DR11 Output Data Bus 14
04	4VODT01	DR11 Output Data Bus 1
05	4VODT13	DR11 Output Data Bus 13
06	4VODT02	DR11 Output Data Bus 2
07	4VODT12	DR11 Output Data Bus 12
08	4VODT03	DR11 Output Data Bus 3
09	4VODT11	DR11 Output Data Bus 11
10	4VODT04	DR11 Output Data Bus 4
11	4VODT10	DR11 Output Data Bus 10
12	4VODT05	DR11 Output Data Bus 5
13	4VODT09	DR11 Output Data Bus 9
14	4VODT06	DR11 Output Data Bus 6
15	4VODT08	DR11 Output Data Bus 8
16	4VODT07	DR11 Output Data Bus 7
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21		not used
22	GND	Ground
23	4VASTSC	Status C
24	GND	Ground
25	4VASTSC	Status C
26	GND	Ground
27	4VASTSB	Status B
28	GND	Ground
29		not used
30	GND	Ground
31	4VASTSA	Status A
32	VCC	10k to VCC
33		not used
34	GND	Ground
35	4VACRDY	Ready
36	GND	Ground
37		not used
38	GND	Ground
39	4VACYRQ	Cycle Request
40	GND	Ground

TABLE 2-11. CONNECTOR LIST		
FRONT PANEL CONNECTOR J03		
MODELS 514V-01 & 514V-02 ONLY		
PIN	SIGNAL	FUNCTION
01	4EDBA00	Channel A Output Bus 0
02	4EDBA01	Channel A Output Bus 1
03	4EDBA02	Channel A Output Bus 2
04	GND	Ground
05	4EDBA03	Channel A Output Bus 3
06	4EDBA04	Channel A Output Bus 4
07	GND	Ground
08	4EDBA05	Channel A Output Bus 5
09	4EDBA06	Channel A Output Bus 6
10	GND	Ground
11	4EDBA07	Channel A Output Bus 7
12	4EDBA08	Channel A Output Bus 8
13	GND	Ground
14	4EDBA09	Channel A Output Bus 9
15	4EDBA010	Channel A Output Bus 10
16	GND	Ground
17	4EDBA011	Channel A Output Bus 11
18	4EDBA012	Channel A Output Bus 12
19	GND	Ground
20	4EDBA013	Channel A Output Bus 13
21	4EDBA014	Channel A Output Bus 14
22	GND	Ground
23	4EDBA015	Channel A Output Bus 15
24	9EDAEOP	Last Word of Buffer
25	4DMARQ0	DMA Request +
26	9DMARQ0	DMA Request -
27	4DMACK0	DMA Acknowledge +
28	9DMACK0	DMA Acknowledge -
29		not used
30	GND	Ground
31		not used
32		not used
33	GND	Ground
34		not used
35	9BUSREN	Bus Read Enable
36	GND	Ground
37		not used
38	GND	Ground
39		not used
40	GND	Ground

TABLE 2-12. CONNECTOR LIST		
FRONT PANEL CONNECTOR J03		
MODELS 514V-03 & 514V-04 ONLY		
PIN	SIGNAL	FUNCTION
01	4VDT15	DR11 Input Data Bus 15
02	4VDT00	DR11 Input Data Bus 0
03	4VDT14	DR11 Input Data Bus 14
04	4VDT01	DR11 Input Data Bus 1
05	4VDT13	DR11 Input Data Bus 13
06	4VDT02	DR11 Input Data Bus 2
07	4VDT12	DR11 Input Data Bus 12
08	4VDT03	DR11 Input Data Bus 3
09	4VDT11	DR11 Input Data Bus 11
10	4VDT04	DR11 Input Data Bus 4
11	4VDT10	DR11 Input Data Bus 10
12	4VDT05	DR11 Input Data Bus 5
13	4VDT09	DR11 Input Data Bus 9
14	4VDT06	DR11 Input Data Bus 6
15	4VDT08	DR11 Input Data Bus 8
16	4VDT07	DR11 Input Data Bus 7
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21		not used
22	GND	Ground
23	4FUNCT1	Function 1
24	GND	Ground
25	4FUNCT1	Function 1
26	GND	Ground
27	4FUNCT2	Function 2
28	GND	Ground
29	GND	Ground
30	GND	Ground
31	4FUNCT3	Function 3
32		not used
33		not used
34	GND	Ground
35	GND	Ground
36	GND	Ground
37	4VAATTN	Attention
38	GND	Ground
39	4VACYBZ	Busy
40	GND	Ground

SECTION 3 OPERATION

3.1 SIGNATURE & CONTROL REGISTERS

The 514V QPOI card receives control signals and transfers setup data via four 16-bit registers. The register addresses are memory-mapped in A16-D16 memory space (first 64kByte page). The register functions are shown in TABLE 3-1, and described in the paragraphs that follow.

Byte Address	Description	Mode
0	Signature	Read Only
2	Command/Status Register	Read/Write
4	DR11 Data Register	Read/Write
6	TA4000 Command/Data Register	Read/Write

TABLE 3-1. Command/Status Registers

The *Signature Register* is a read only register the program checks to determine if there is a QPOI card installed. The register contains the hexadecimal value 0514. The uppermost nibble is switch-configurable. The *Command/Status Register* and *DR11 Data Register* are discussed below.

3.2 OPERATION

The QPOI provides four separate output channels. Selector switches enable you to select between several individual output channel options, as well as individual selection of the Device Bus *output device number* that the 32 bit and 16 bit channels A & B will respond to. Channel C is a special purpose channel that responds to device 7. These switch settings are explained in Section 5.

3.2.1 Data Transfer to The 32 Bit Parallel Output

You can use this channel as a general purpose channel to transfer data and address as a 32 bit message to an external device. The system contains algorithms for a variety of output devices. You must insure that the output format of a specific algorithm is compatible with your intended use. You can set the device address to 7 to allow the channel to function as an external DAC bus, which normally interfaces the TDP to external DAC converters and discrete line circuits such as our Model 2240 chassis. Device 7 is supported with special algorithms for analog and discrete line outputs - and to provide the required message format. The QPOI hardware interfaces the device bus to the DAC bus, where the QPOI captures ID and Data addressed to Device 7. The data consists of a 16 bit word, while the ID word contains 12 address lines plus four lines that configure the receiving hardware. These 32 lines, along with three control signals, are buffered and connected to the P2 connector of the 514V card. The pin numbers and signal functions are listed in TABLE 2-11 of Section 2.

Switch selectable speeds allow transfers from 0.8 to 2.2 megawords per second. FIGURES 3-1 through 3-7 (pages 3-8 to 3-11) contain the timing diagrams for high and low rate transfers. A word transfer is initiated by the Digital to Analog Address Enable signal 9DACAEB, which is set to 0 when the address is output

on the bus. The external hardware can extend the transfer cycle by setting WAIT signal 9DACWAT to **0** if the external device is not ready for the data word. When wait is set to **1** the data strobe signal 9DATSTB will be set to **0** to complete the data transfer cycle.

3.2.2 Channel A Data Transfer to Host

The host computer data bus can also transfer selected data from the TDP output device bus (controlled by the 504VA and 505V cards) to the host computer. Bit 0 must be set to **1** of the CSR to enable channels A, B, & C. See Figure 3.1. The host data bus signals 4CHAD00 through 4CHAD15 are HIGH asserted signals. 00 is the least significant bit and 15 is the sign bit. The data is transferred to the host computer memory by a DMA channel located in the host computer. The TDP digital data processing algorithms provide for outputting to four *devices*, with each device providing up to four ports (or channels). The two bits which specify the Port are derived from bits stored in the TDP's distribution memory by the setup program; hence they are user programmable. 16 bits of data and an EOP flag are loaded into a 2k FIFO via the A-Bus. When data is ready out of the FIFO, request signal 9DMARQO is set to **0** to indicate the availability of a data word for the host. The Host interface is free to use this signal to qualify the data in any way required by the specific application. Acroamatics does not assign any particular meaning to these channel qualifiers. When the host is ready to accept the data, lines 9BUSREN and the channel acknowledge line 9DMACK0 are set to **0** by the host. This enables the data onto the host data bus (4CHAD00-15). The host samples the data, 9DMACK0 and 9BUSREN are set to **1** to complete the cycle. When the acknowledge is received the interface sets request to **1** unless another word is ready to be output. If a second word is ready at the FIFO output (when the acknowledgement for the first word is received) the request signal remains set to **0** and the next word is made available at the output bus as soon as the acknowledge for the first word returns to **1**. The host must reassert the acknowledge when it is ready to accept the second word. A maximum of eight consecutive DMA transfers can occur before releasing DMA Request. FIGURE 3-3 shows the timing for a single word transfer and FIGURE 3-4 shows a burst transfer of consecutive words to the same DMA channel. A Timing Diagram shows the signal relationships for both a single word transfer and an instance when the channel is ready to transfer another word at the completion of the current word transfer. (The single word transfer timing applies if the transfer is to the other channel.)

Another control line in the host interface is signal 9TDAEOP which is used in conjunction with a DMA controller circuit to allow the host DMA to detect *End of Buffer* when the TDP reaches *End Of Process*. The End of Process flag is controlled by special algorithms that allow the last word of a frame or record to terminate the current input buffer.

3.2.3 Channel B Data Transfer to Host

Channel B is for directly transferring selected data into two hardware registers in the host computer. You can load data into either or both registers, specified by the user programmable port bits controlled by the data processing algorithms. 19 bits of data and control flags are loaded into a 2k FIFO via the A-Bus. The host data bus signals 4CHBD00 through 4CHBD15 are HIGH asserted signals. This channel also provides low asserted, algorithm-controlled signal 9TDBEOP. This signal is normally set to 0 at the end of either a PCM frame or an End of Record Count, and used by the external hardware to indicate an End of Process. The signals that control the transfer to channels 1 and 2 (derived from the port bits) are differential RS-422 compatible signals. When a word is ready for transfer, the Channel Ready signal (or both Channel Ready signals for a dual transfer) are tested. When ready, a 62ns output strobe is generated to the appropriate channel(s). FIGURE 3-5 is a timing diagram for channel B.

3.2.4 Channel C Data Transfer to TA4000 SCRS

Channel C is a special channel that takes data addressed to *device 7* (the DAC Bus) when address line 7 set to 1 (addressing DAC channels 128 through 255), and reformats the data messages for output on channel C. It's data is also buffered through a 2k FIFO. This block of 128 DAC channels are reserved for TA4000 use when using Channel C. The address portion of the DAC message and the *discrete line selector* (bit 12) together format a message that addresses a specific channel in the TA4000 recorder. The TA4000 has a unique *recorder address* that is selectable with dip switches located on the TA4000 CPU board. The TA4000 contains up to three plug-in modules, selected by the module address, each with eight addressable channels (channel address). The output message is accomplished by a two word transfer, with the first word providing the *address* of the selected channel, and the second the 12-bit data value for analog channels (or a one/zero for discrete line messages). The formats of these messages are shown in TABLE 3-3 below.

COMMAND/STATUS REGISTER (Address 02)		
BIT	FUNCTION	MODE
0	Host Interface enable	R/W

TABLE 3-2. Command/Status Register

3.2.5 TA4000 Command/Data Register (Address 06)

TA4000 MESSAGE FORMATS							Description	
15	12	11	8	7	4	3	0	
0	0							Transfer is Data
	x	x						Module Address *
		x						Sign Bit
			x	x	x	x	x	Data (trace deflection)
1	1	0	0					Transfer is Address
		x	x	x	x			Recorder Address
					x	x		Module Address
						x	x	Channel Address
1	1	1	1					Transfer is Discrete Line
		0	0	0	0	0	0	Always Zero
							x	Marker (One = ON)

* May be "don't care" bits, depending upon plug-in module jumper selection.

TABLE 3-3. TA4000 Message Formats

The bus to the TA4000 is 18 lines wide. There are 17 outputs and one input. Sixteen lines, as outputs, carry Address, Data, or Event markers. A strobe, set to **0** for 500ns, is output after 100ns of setup time for the sixteen lines. The TA4000 returns a busy before the strobe finishes. The interface must wait until the busy is set to **1** before driving the strobe line again.

The uppermost nibble of the sixteen lines is unique for each of the three types of transfers. The uppermost nibble for *addresses* is 1100, *data* is 00xx (where xx is the two bit module address repeated in the data word), and *discrete line* is 1111.

Transfers to the TA4000 can also originate at the host computer. These messages are transferred via the VMEbus using a register at a switch selectable address in the VME A16-D16 memory. The message format is as shown in TABLE 3-3. First the address is loaded by the uppermost nibble set to 1100. Next the data is loaded with the uppermost nibble set to 00xx. The message is then sent out on the TA4000 bus.

3.3 DR11 INTERFACE

The DR11W interface provides a communication path between the Acroamatics Model 2200 series VME Telemetry Data Processors and a Digital Equipment Corporation VAX or PDP series computer that is equipped with a DR11W or DRV11W interface, or to any computer which has an interface which emulates one of these, as shown in the following table.

INTERFACE CONFIGURATIONS	
SYSTEM	MODE
VAX	DR11-W
VAX-11 UBA	DR11-W
PDP-11	DR11-W
UNIBUS-11	DR11-W
MicroVAX	DRV11-WA
Q BUS-11	DRV11-WA
LSI-11	DRV11-WA
LSI-11 BUS	DRV11-WA
<i>The terms VAX™ and MicroVAX™ are registered trademarks of DEC.</i>	

TABLE 3-4. Interfaces Supported by the QPOI

The interface supports a bi-directional channel for data transfer and setup information. Control information is exchanged between the TDP and the host computer via function and status lines. The remainder of this section discusses the interface signals and timing requirements. The interface signal connections at the TDP rear panel and the pin allocations for these signals are given in Section 2.

3.3.1 Setup and Control

Internal signals control information transfer between the TDP and the host computer. Setup information and run/stop commands are received by interpreting function lines. The TDP host processor manages this exchange. Setup is initiated by the host CPU selecting the channel for output. This is accompanied by setting function line one to **0** (4VAFUN1), indicating that data transfer is to the TDP. Channel Ready (4VACRDY) will be set to **0** causing the TDP to initiate the first data request (4VACYRQ), and DMA cycle busy (4VACYBZ) will load the output data (4VODT00) through (4VODT15) into the data register on the interface when the DMA cycle is complete (trailing edge of 4VACYBZ loads data). Register full flags allow the orderly flow of information from the external computer to the TDP for program setup. Each time the host processor reads the data register, the next data word is requested via the host DMA channel. The host may control the setup sequence by asserting attention (4VAATIN) and asserting input data request status line (4VTDSTA) to indicate that a data transfer to the host is required. The host will then re-enable the DMA channel with function line one (4VAFUN1) set to **1**. The host then loads the data register, which then transfers the data to the host via the DMA channel. Input cycles are described in the following paragraph.

The following table describes the host interface registers as they are used in the DR11 interface.

DR11 COMMAND/STATUS REGISTER (Address 02)		
Bit	Function	Mode
0	Status Bit C	R/W
1	Status Bit B	R/W
2	Status Bit A	R/W
3	Reset Interface	W
3	Function Bit 1	R
4	Function Bit 2	R
5	Function Bit 3	R
8	Data FIFO not Empty	R
9	Set Attention	R/W
10	Data Input Register Full	R
12	Data Output Register Full	R
13	Channel Not Ready To Transfer	R
13	Backstrap Test Mode	W
Bits 6, 7, 11, 14, 15 not used		

TABLE 3-5. DMA Command/Status Register (Address 02)

DR11 DATA REGISTER (Address 04)		
Bit	Function	Mode
0-15	Input Data from DR11	R
0-15	Output Data to DR11	W

TABLE 3-6. DR11 Data Register (Address 04)

3.3.2 DR11 Function Commands

The three bit function field which can be controlled by the PDP-11 (or VAX) computer is interpreted by firmware in the TDP.

The functions have been defined by firmware. Not all of the functions which are defined here are implemented in all units. The setup functions and data acquisition functions (marked with an *, below) are standard features. The function commands permit character data to be transmitted either byte swapped in the 16 data field or not byte swapped. The TDP will either byte swap or not byte swap its reply depending on the mode in which the setup information is transmitted. This consideration applies only to the exchange of setup information. The data stream is always 16 bits wide and is never byte swapped. The following table lists the implemented function commands.

Code	Function	Standard
0	Send Setup (Byte Swapped)	*
1	Receive Reply	*
2	Send Setup (Not Byte Swapped)	*
3	Receive Data, RUN TDP	*
4	Send Task Request (Swapped)	
5	Receive Data, STOP TDP	*
6	Send Task Request (Not Swapped)	
7	Receive Input Buffer Contents	*

Functions 4 and 6 are provided to permit custom software to be implemented in the TDP. this permits the Host computer to command special function tasks. Functions 3 and 5 are used to receive the processed data stream on channel A. Function 3 must be used as long as the TDP is to be kept in the RUN Mode. Function 5 is used to stop the TDP and at the same time receive the final data buffers from the FIFO. Function 7 is intended for self-test. The contents of the input buffer as received from the Host Computer using functions 0, 2, 4, or 6, is retransmitted back to the Host. If the buffer sent from the host begins with a binary word containing all ones (integer -1), the TDP will not process the buffer, but will assume that it is a test buffer. Then Function 7 can be used to read the buffer back to verify that the communication channel is working properly.

3.3.3 DR-11 Status Bits

The three status bits inform the host computer of the TDP operating state. The bits are called A, B, in C, and in the document will be referred to as **ST A**, **ST B**, and **ST C**. **ST A** = 1 indicates that the TDP is in remote mode. Bits B and C are encoded as follows:

B	C	
—	—	
0	0	TDP Busy Processing Input.
0	1	TDP Ready for Input
1	0	TDP Ready for Input, previous input had transmission errors
1	1	TDP Ready for Input, previous transmission had logic errors

For transfers of setup information, only codes 0 and 1 have meaning. Codes 2 and 3 are used to control the processing of special task messages(transmitted with function codes 4 and 6) for custom applications.

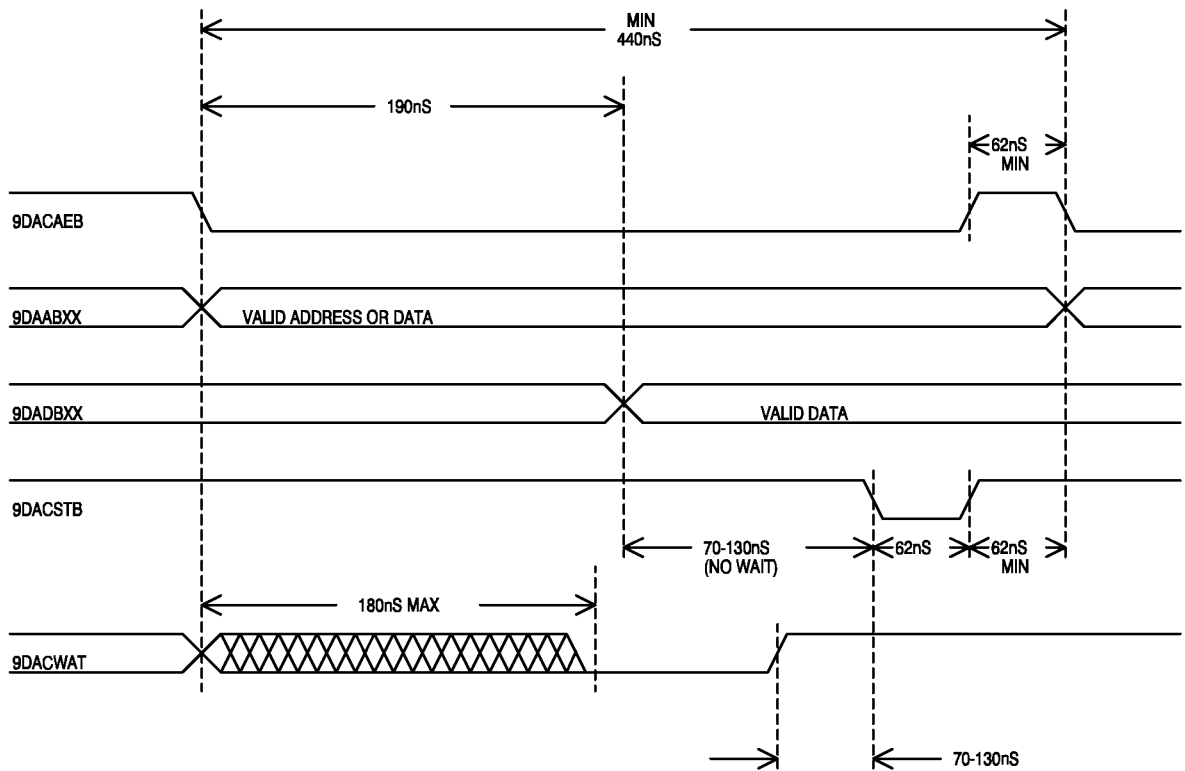


FIGURE 3.1 (FAST CYCLE)

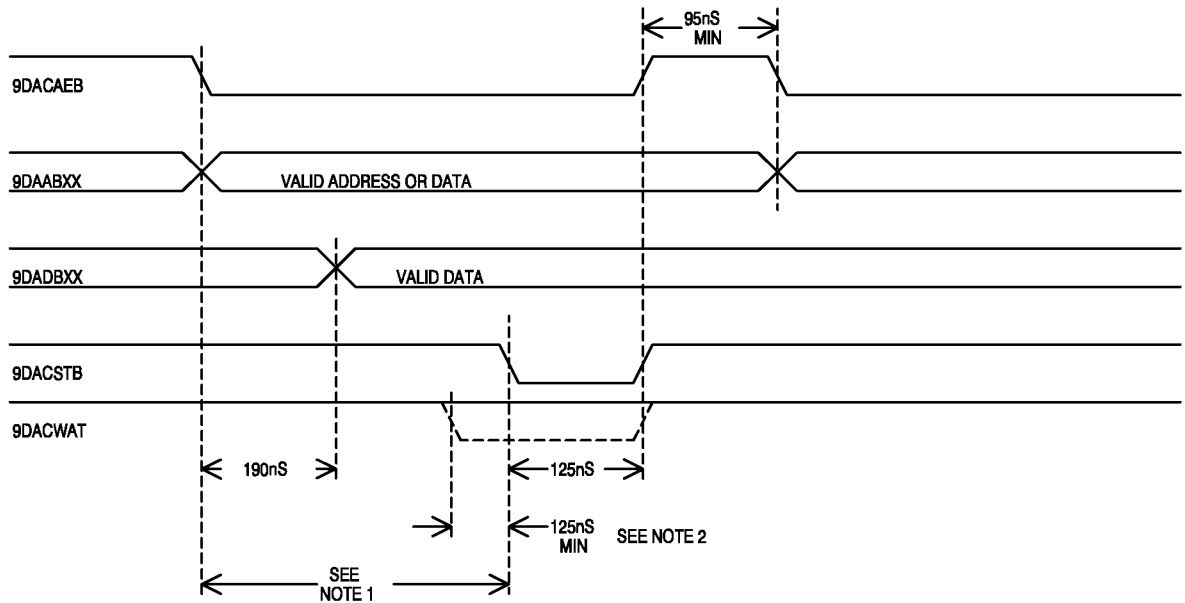


FIGURE 3.2 (SLOW CYCLES)

NOTES: 1) SWITCH SELECTABLE DELAY:

MODE DELAY	1	2	3
	460-520nS	700-760nS	940-1000nS

2) WAIT IS SAMPLED AT END OF DELAY.

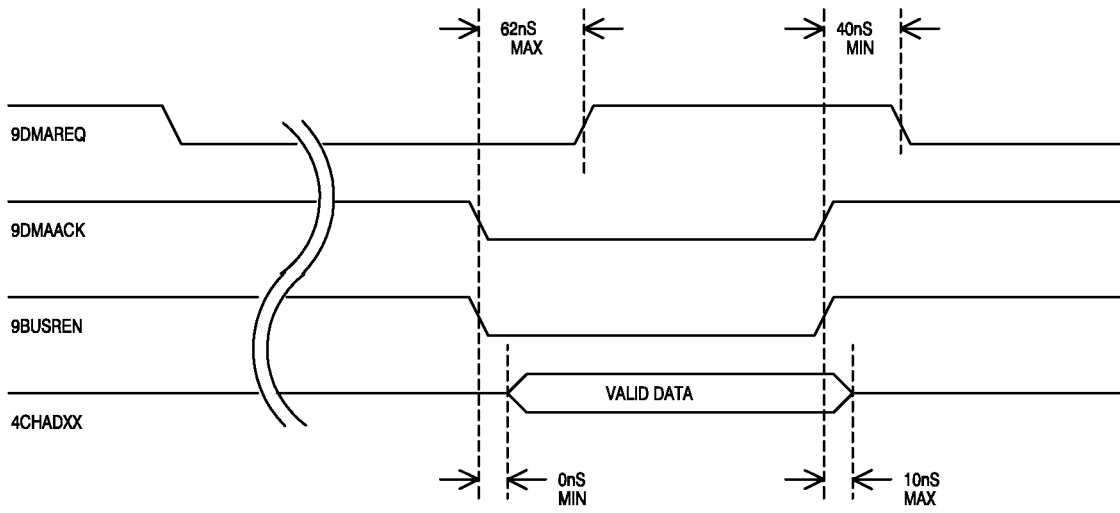
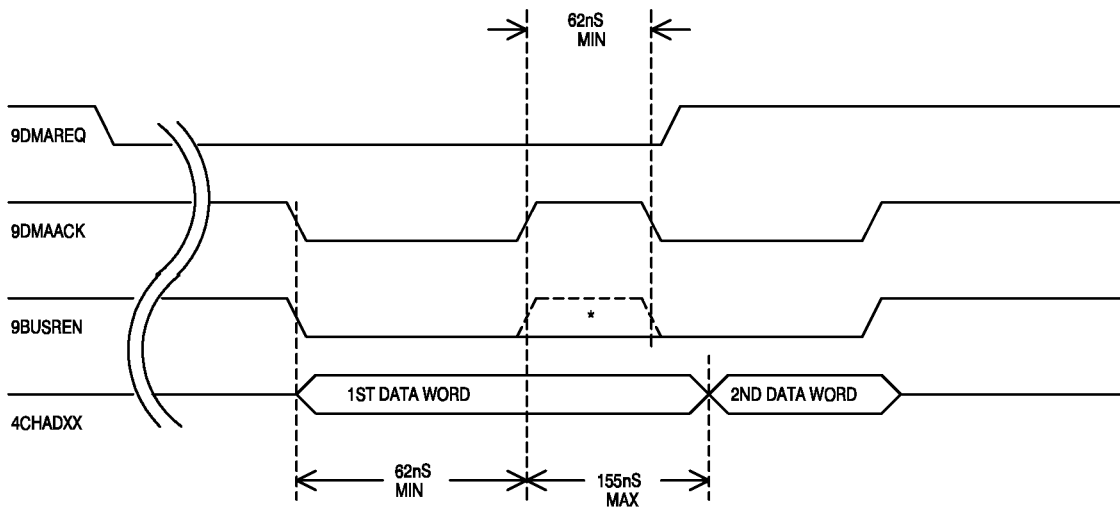


FIGURE 3.3 (SINGLE CYCLE)



* 9BUSREN CAN STAY LOW DURING MULTIPLE CYCLES.

FIGURE 3.4 (MULTIPLE CYCLE)

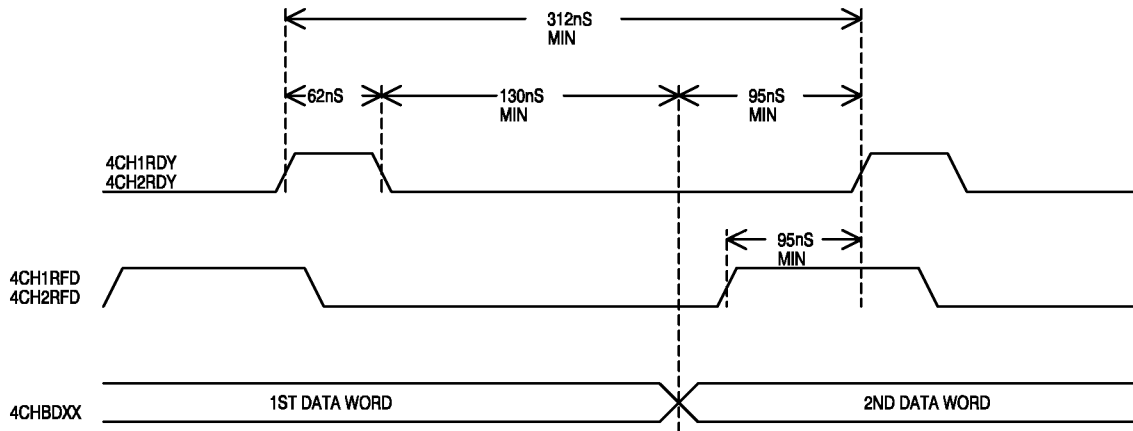
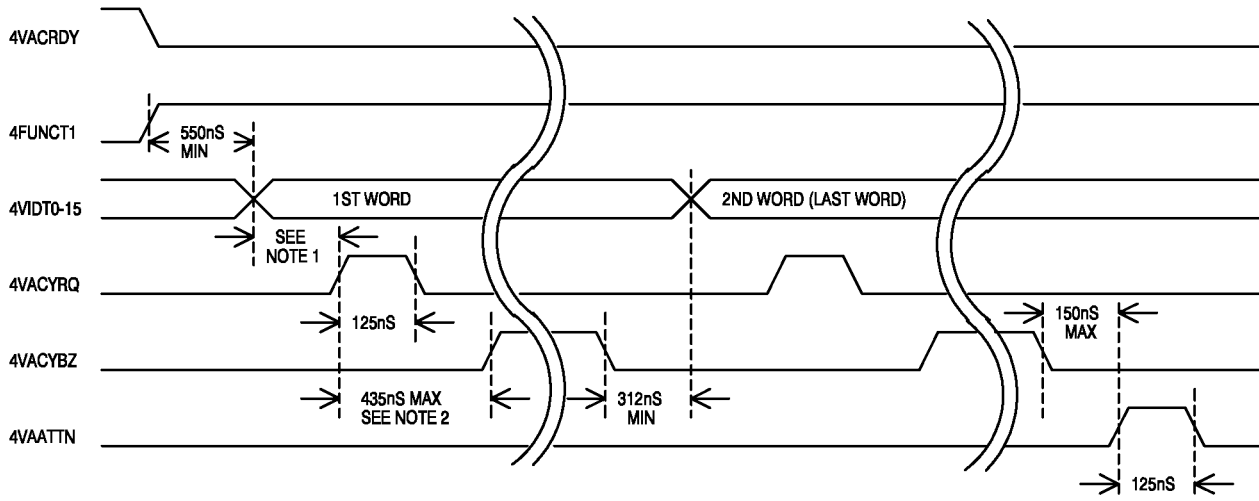
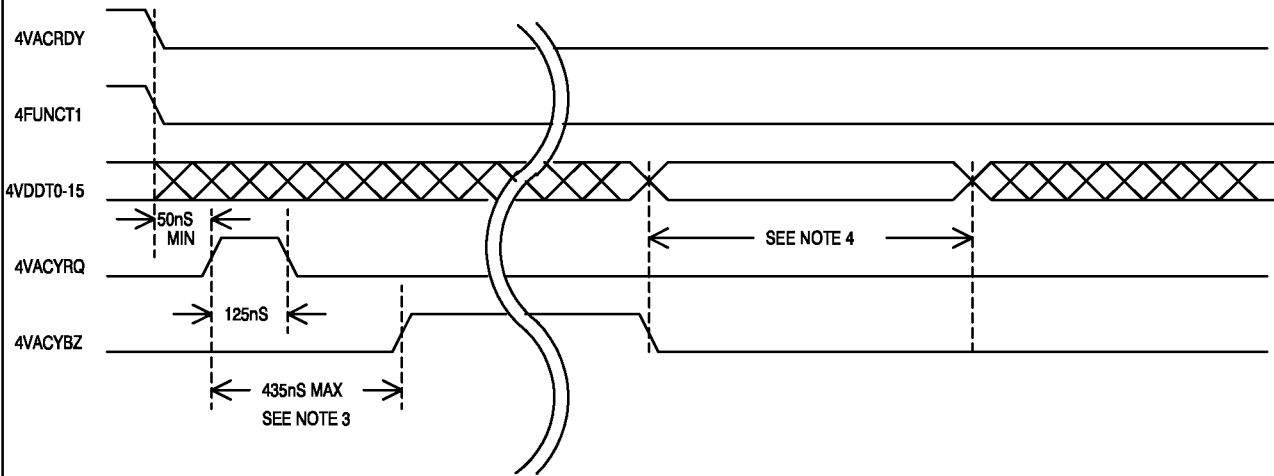


FIGURE 3.5 (CHANNEL B)



DR11 OUTPUT CYCLE
FIGURE 3.6



DR11 INPUT CYCLE
FIGURE 3.7

NOTES: 1) SWITCH SELECTABLE DELAY:

MODE	1	2	3	4
DELAY	125nS	375nS	625nS	875nS

2) THE INTERFACE EXPECTS A BUSY REPLY WITHIN 435nS. IF THIS IS NOT MET, A BUS TIMEOUT WILL OCCUR AND THE DATA IS EFFECTIVELY THROWN AWAY.

3) THE INTERFACE EXPECTS A BUSY REPLY WITHIN 435nS. IF THIS IS NOT MET, A BUS TIMEOUT WILL OCCUR AND THE INTERFACE WILL ATTEMPT ANOTHER TRANSFER.

4) DATA HOLD TIMES MUST BE MET FOR THE SELECTED MODE.

MODE	1	2	3	4
HOLD TIME	340nS	590nS	840nS	1090nS

3.3.4 Data Transfer to Host Computer

The host computer data input bus transfers selected data from the TDP output data bus (controlled by the 505V Programmable Data Stream Processor card) to the host computer. The data is buffered by a 2048 word FIFO memory to provide smoothing of the host interrupt latency time between DMA records of high rate telemetry data.

The host data bus signals 4VDTI00 - 4VDTI15 are HIGH asserted signals with 00 being the LSB and 15 the sign bit. The input transfers are initiated by the host by setting function 1 to **0** and setting signal 4VACRDY to **0**. Once data is available at FIFO memory output, cycle request signal 4VACYRQ is set to **1** which results in DMA cycle busy signal 4VACYBZ being set to **1**. Signal 4VACYBZ returning to **0** indicates the output cycle is complete. The host computer may stop the TDP by setting function five with the last record that is to be input. The TDP reads the function lines, selects TDP IDLE mode, and sets attention line 4VAATTN to **1** to inform the host that the TDP is in IDLE mode.

MODEL 514V QUAD PARALLEL OUTPUT I/F SPECIFICATIONS

DEVICE BUS (INPUT)	All signals are single ended TTL levels
16 Data	All signals are High asserted. Line 0 is LSB, line 15 MSB (SIGN).
8 Control	High asserted control lines provide 2 port lines, 3 device lines, and an End of Transfer signal. Low asserted control lines provide a Last Word of Message flag, a Data Strobe, a Reset, and an open collector Wait line.
Max Transfer Rate	4.6 megawords per second sustained.
32 BIT PARALLEL OUTPUT CHANNEL	All signals are single-ended TTL levels, LOW asserted. The 12 LSBs are always ID (although not all lines may be active)
16 Data	Line 0 is LSB, line 15 is MSB (SIGN).
16 Address	Line 0 is LSB, line 15 MSB.
Address Enable	Set LOW when address is loaded (used to set Wait on low rate channel).
Wait	Set LOW to delay data transfer.
Data Strobe	Strobes the transfer of Address and Data
Transfer Rate (max)	Switch selectable, 0.8 to 2.2 mega-transfers per second sustained.
16 BIT CHANNEL A OUTPUT	All signals are single ended TTL levels except for DMA Request and Grant for DMA0 which are complementary RS-422 levels.
16 Data	All signals are HIGH asserted. Line 0 is LSB and line 15 is MSB (SIGN).
Control	DMA0 Request and Grant are complimentary TTL signals. End of Process is a single ended LOW asserted signal.
Transfer Rate (max)	4.6 Megawords ps sustained.
16 BIT CHANNEL B OUTPUT	All signals are single ended TTL levels except for transfer controls, which are complementary RS-422 levels.
16 Data	All signals are HIGH asserted. Line 0 is LSB and line 15 is MSB (SIGN).
Control	End of Process is a single ended, LOW asserted, TTL level signal. Transfer controls for channel 1 and 2 are complimentary RS-422 signals.
Transfer Rate (max)	3.2 Megawords ps.
16 BIT CHANNEL C OUTPUT	All signals are single ended TTL levels. Words are addressed to Device 7 (the DAC Bus) and reformatted as required by the TA4000.
16 Data	All signals are HIGH asserted. Line 0 is LSB and line 15 is MSB (SIGN). Three types of messages are transferred as indicated by the four MSB of each output word.
Control	Low asserted Ready from TA4000, and LOW asserted Strobe from Channel C.
Transfer Rate (max)	Limited by TA4000. Burst channel rate is one megaword per second.

REQUIREMENTS

Power	+5VDC at 1.7 Amp
Temperature	Operating: 0 to +40°C, Non-Operating: -40 to +86°C
Relative Humidity	Up to 90% non-condensing
Air Flow	30 Linear FPM
Shock	Operating: 6G, Non-operating: 50G
Vibration	Operating: 0.5G, 5 to 2000, Non-operating: 1.2G, 5 to 500

Specifications are subject to change without notice.

SECTION 4 THEORY OF OPERATION

4.1 BLOCK DIAGRAM

This chapter contains a block diagram of the QPOI card.

SECTION 5 ADJUSTABLE SWITCH & JUMPER SETTINGS

5.1 DESCRIPTION

The paragraphs below describe the selections available on the Model 514V Quad Parallel Output Interface card.

5.1.1 U14, U16 - Address Select

U14 and U16 select the base of the eight byte block of QPOI registers in the A16:D16 address space A3 through A15. U16 switches 1-8 select the eight MSBs, and U14 switches 1-5 select the five LSBs.

5.1.2 U13 - Port Output Options

Switches 1-5 of U13 select the options for the DR11 interface (card model 514VA/DR) and the DAC bus. Switches 6 & 7 are read into the Signature Register. The switch selections available are shown on page 5-3.

5.1.3 U5 - A Bus Device Selection

Each output port can respond to a selectable output device number, which is addressed by switches 1-7 of U5. Selections are shown on page 5-3.

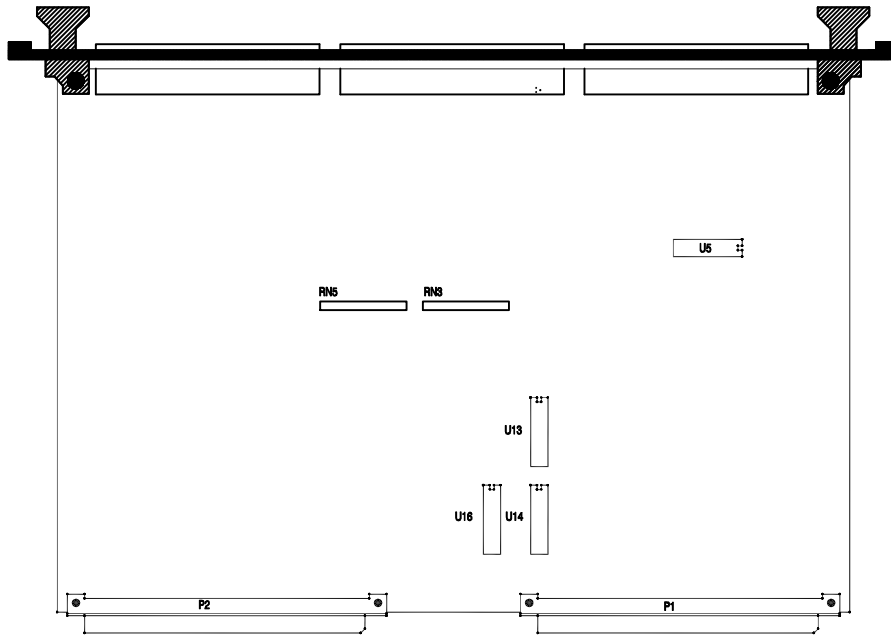
5.2 DR11 DEVICE CONFIGURATION

5.2.1 DR11-W Mode

1. U13 - switch S6 must be OFF, and S1 must be ON.
2. SIP resistors RN3 & RN5 must be *inserted* as shown on page 5.2.
3. Select the appropriate transfer mode with switches 2 & 3 of U13.

5.2.2 DRV11-WA Mode

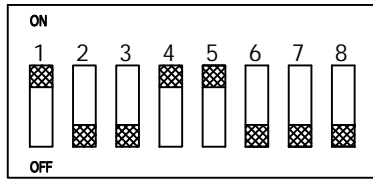
1. U13 - switches S6 and S1 must be OFF.
2. SIP resistors RN3 & RN5 must be *removed*.
3. Select the appropriate transfer mode with switches 2 & 3 of U13.



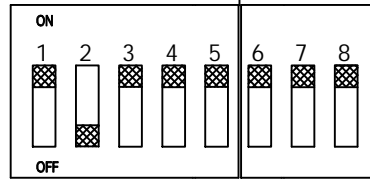
ADDRESS 6740 SHOWN

A15 ← A3

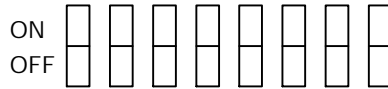
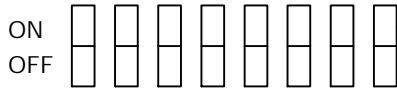
ON = 0
OFF = 1



U16



U14



SHIPPED ADDRESS _____

CARD 6011514

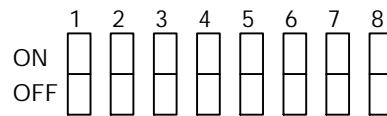
SERIAL# / REV. _____

CUSTOMER _____ JOB# _____

CONFIGURED BY _____ DATE _____

QC CHECK BY _____ DATE _____

SWITCH U5



SWITCH U13

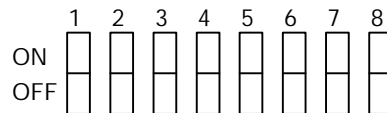


FIGURE 5-1. QUAD PARALLEL OUTPUT INTERFACE (QPOI) FACTORY SETTINGS.

SWITCH U5		SCU Ch. A OR DR11
1	2	DESCRIPTION
OFF	OFF	DEVICE 0
OFF	ON	DEVICE 1
ON	OFF	DEVICE 2
ON	ON	DEVICE 3

SWITCH U13			DR11 OPTIONS
1	2	3	DESCRIPTION
ON	X	X	DR11-W MODE
OFF	X	X	DRV11-WA MODE
X	ON	ON	DELAY MODE 1*
X	ON	OFF	DELAY MODE 2*
X	OFF	ON	DELAY MODE 3*
X	OFF	OFF	DELAY MODE 4*

* SEE TIMING DIAGRAM 3-6 & 3-7

SWITCH U5		SCU Ch. B
3	4	DESCRIPTION
OFF	OFF	DEVICE 0
OFF	ON	DEVICE 1
ON	OFF	DEVICE 2
ON	ON	DEVICE 3

SWITCH U13		DAC BUS OPTIONS
4	5	DESCRIPTION
ON	ON	FAST CYCLE (see Fig. 3-1)
ON	OFF	SLOW CYCLE MODE 1*
OFF	ON	SLOW CYCLE MODE 2*
OFF	OFF	SLOW CYCLE MODE 3*

* SEE TIMING DIAGRAM 3-2.

SWITCH U5			DAC BUS
5	6	7	DESCRIPTION
OFF	OFF	OFF	DEVICE 0
OFF	OFF	ON	DEVICE 1
OFF	ON	OFF	DEVICE 2
OFF	ON	ON	DEVICE 3
ON	X	X	DEVICE 7

SWITCH U13		SIGNATURE REGISTER
6	7	DESCRIPTION
ON	ON	SIG 0514, SCU I/F, TA4000 I/F
ON	OFF	SIG 1514, SCU I/F ONLY
OFF	ON	SIG 2514, DR11 I/F, TA4000 I/F
OFF	OFF	SIG 3514, DR11 I/F ONLY

CARD # 6011514

FIGURE 5-2. QUAD PARALLEL OUTPUT INTERFACE (QPOI) SELECTIONS

SECTION 6 DRAWINGS

6.1 INTRODUCTION TO THE DRAWINGS

Section 6 contains a complete technical drawing package describing your VME card. The drawings in this section are keyed to your specific serial numbered card.

6.1.1 Drawing System

Acroamatics Drawing numbers are seven digit numbers which can also have a two digit dash number. The first four digits represent a drawing class, and wherever a drawing may be part of a standard drawing package, drawing numbers are issued so that all drawings which are part of the package share the same last three digits. In the following discussion "xxx" represents the number keyed to the the card part number (6011xxx). Individual parts are classified within the same drawing system, but are assigned serially without regard to other assemblies.

The PC Card Reference package includes the following drawings:

FOR CARD PART NUMBER 60115xx:

60115xx	Card Assembly Drawing
81115xx	Card List of Materials
21115xx	Card Schematic Drawing

6.1.2 Drawing Package Organization

This section of the manual contains the physical drawings, called *Drawings*, as opposed to the schematic drawings, called *Schematics*, which are found in Section 7.

The Drawings section includes the card component assembly drawing 60115nn and the card List Of Materials (LOM). LOM's include sufficient information to facilitate ordering replacement parts either from Acroamatics or from the original component manufacturer. LOMs list parts by Acroamatics Part Number in the column headed *PART NO.* The component manufacturer is identified as *VENDOR.* Parts for which ACROAMATICS is listed as vendor are proprietary components available only from Acroamatics, Inc. Integrated Circuits which are industry standard are listed as *GENERIC*, and may be obtained from any reliable vendor. Other parts for which a specific source is listed may be available from other sources. When substituting parts from vendors other than those specifically listed, be certain that the components are truly interchangeable.

The last column (Reference) of the List of Materials lists the assembly location or locations. An assembly location can contain a socket as well as the component plugged into the socket.

For example

U15
S1
74ALS244

This example shows that location U15 contains socket S1 and an IC of type 74ALS244. Resistors, capacitors, and other components are shown in a similar fashion, and are referenced using common industry abbreviations.

6.1.3 Programmed Parts

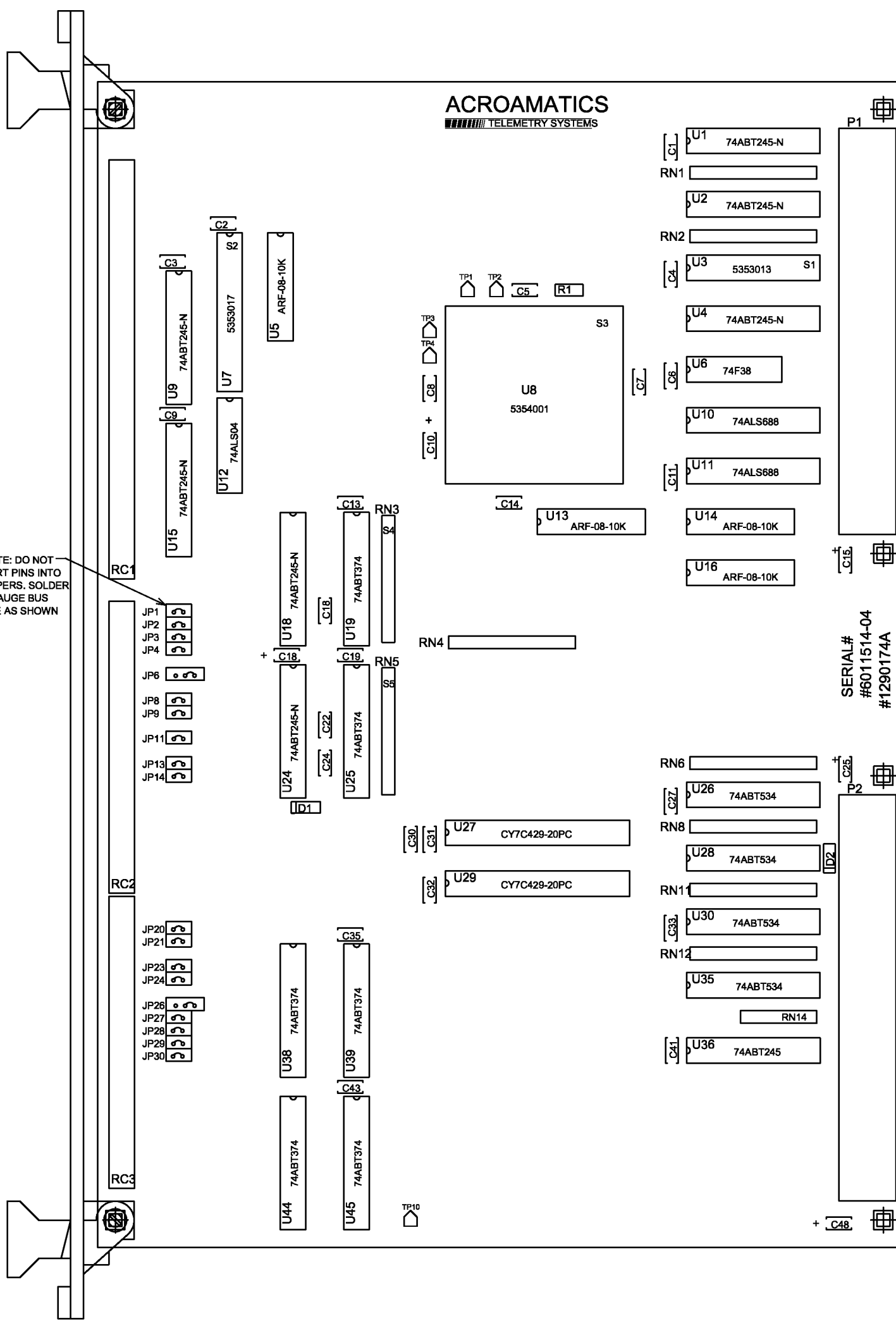
The VME card can include programmed parts such as PROMs, EPROMs, EEPROMs, PALs, GALs, FPGAs, etc. If these are a permanent part of the hardware, they are documented on the List Of Materials for the PC card on which they are installed. Programmed parts are listed on the LOM twice; once as the unprogrammed part, with the Manufacturers Part Number, and also under the Acroamatics program number (606xxxx) with which they must be programmed to become the correct programmed part.

Programs for PROMs have part numbers in the series 6061xxx

Programs for EPROMs and EEPROMs have part numbers in the series 6062xxx

Programs for PALs and GALs have part numbers in the series 6064xxx

Programs for FPGAs have part numbers in the series 6067xxx



NOTE: DO NOT INSERT PINS INTO JUMPERS. SOLDER 24 GAUGE BUS WIRE AS SHOWN

ACROAMATICS
TELEMETRY SYSTEMS

SERIAL#
#6011514-04
#1290174A

DR	D MACDONALD	8/04	ACROAMATICS <small>TELEMETRY SYSTEMS</small> GOLETA, CAL. 93117		
CHK					
A P P D			ASSEMBLY, CIRCUIT CARD VME QPOI (DR11 W/O TA4000)		
NEXT ASSY	USED ON		SIZE	SCALE	DWG NO.
			B	NTS	6011514-04
APPLICATION			SHEET	2 OF 2	REV C

LIST OF MATERIALS **8111514-04**
VME PRL INTF(DR11 w/oTA400)

ASSEMBLY PN 6011514-04

DRAWN BY bryan

Mar 14 2001

REVISION C

ENGINEERING APPROVAL _____ DATE _____

MANUFACTURING APPROVAL _____ DATE _____

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
1	1290174	1	PCB VME QPOI	1290174	ACROAMATICS	
2	2796061	2	CONN PC 96P SDR RTANGL	7296-50C2TH	3M	P1,2
3	2796059	1	CONN PC 60P SDR RTANGL	2560-5002UB	3M	RC1
4	2796038	2	CONN PC 40P SDR RTANG 4W HDR	2540-5002UB	3M	RC2,3
5	8542072	1	SOCKET 20-PIN LOPRO .3w	115-93-320-41-003	PRECI-DIP	S1
5			Acceptable substitute is:	DIP-050-320-160-B	MCKENZIE	
6	8542073	1	SOCKET 24-PIN LOPRO .3w	DIP-050-324-160-B	MCKENZIE	S2
6			Acceptable substitute is:	115-93-324-41-003	PRECI-DIP	
7	8542079	1	SOCKET 84-PIN	PD-540-99-084-24-0	0 PRECI-DIP	S3
8	8542047	1	SOCKET 20-PIN STRIP IN-LINE	SS-120-G-2	SAMTEC	S4,5(2-10 PIN)
9	1902161	2	CAP CERM 100pF 50V	CN15C101J	CENTRALAB	C20,30
10	1902169	3	CAP CERM 1000pf 200V 10%	C315C102K2R5CA	KEMET	C16,22,24
11	1902055	20	CAP CERM .1uF 50V .2" LS	C322C104M5R5CA	KEMET	C1-9,11,13,14,19,27,31-33, 35,41,43
11						
12	1922611	5	CAP TA EPXY 4.7uF 10V	T368A475M010AS	KEMET	C10,15,18,25,48
13	7672037	1	RES 10K OHM 1/4W 5% CARBON	GENERIC	GENERIC	R1
14	7700036	6	RES SIP 1.5K/3.3K 10P 2%	CSC10A05-152/332-G	DALE	RN3,5,6,8,11,12
15	7700050	1	RES SIP 1.5K/3.3K OHM 6P	CSC06A-05-152/332J	DALE	RN14
16	7700026	3	RES SIP 10K 9RES 10-PIN	L10-1-103	BECKMAN	RN1,2,4
17						
18	5300004-30	1	IC HEX INVERTER	74ALS04	GENERIC	U12
19	5300038-38	1	IC QUAD 2-INP NAND BUFFER OC	74F38	GENERIC	U6
20	5300245-48	8	IC OCT BUS XCVR .3DIP NI TS	74ABT245N	GENERIC	U1,2,4,9,15,18,24,36
21	5300374-48	6	IC OCT D-F/F TS DIP	74ABT374	GENERIC	U19,25,38,39,44,45
22	5300534-48	4	IC OCTAL D-LATCH, INVERTED	74ABT534N	SIGNETICS	U26,28,30,35
23	5300688-30	2	IC 8-BIT MAG COMP	74ALS688	GENERIC	U10,11
24	5308429-20	2	IC 2K x 9 BIT FIFO	CY7C429-20PC	CYPRESS	U27,29
25	5353013	1	IC PAL/GAL 16V8 10ns	GAL16V8A-10LP	LATTICE	UNPROGRAMMED GAL
26	5353017	1	IC GAL 22V10 10ns 24P	GAL22V10B-10LP	LATTICE	UNPROGRAMMED GAL
27	5354001	1	FPGA 2000 GATE PLCC	A40MX04-PL84	ACTEL	UNPROGRAMMED FPGA
28	6064309	1	QPOI A-BUS INTERFACE	5353017-REV.A	ACROAMATICS	U7
29	6064310	1	QPOI VME DECODE	5353013-REV.A	ACROAMATICS	U3
30	6067054	1	VME QPOI 3 PORT INTERFACE	5354001-REV.B	ACROAMATICS	QPOI7054, U8
31						
32						
33	3573819	2	DIODE SCHOTTKY SWTCH 10ns 1A	1N5819	MOTOROLA	D1,2
34	9070011	4	DIP SWITCH 8-POS W/10K RES PU	ARF-08-10K	ALCO	U5,13,14,16
35	9250004	1	TERM W-W PINS PKG OF 160	86090-4	AMP.	5 USED
36	5600012	1	LABEL,VME PNL, ACRO	5600012	ACROAMATICS	
37	5600026	1	LABEL,VME PNL, QPOI	5600026	ACROAMATICS	
38	6730092	1	FR PNL-VME BLANK	6U4EF0000	TRIPLE-E	SCRN #8071172 MOD #5951104

