

DN 6000331

TECHNICAL MANUAL
MODEL 505VA

• PROGRAMMABLE DATA STREAM PROCESSOR •

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TABLE OF CONTENTS

SECTION 1	INTRODUCTION	1-1
1.1	DESCRIPTION	1-1
1.1.1	Multiple Algorithms	1-1
1.1.2	Derived Parameters	1-1
1.1.3	Output Formatting	1-1
1.2	OPTIONS	1-2
1.3	DOCUMENT CONVENTIONS	1-2
SECTION 2	INSTALLATION	2-1
2.1	GENERAL	2-1
2.2	UNPACKING	2-1
2.3	FACTORY RETURN	2-1
2.4	INSTALLING	2-1
2.5	CONNECTORS	2-3
SECTION 3	OPERATION	3-1
3.1	GENERAL	3-1
3.2	PDSP MEMORY MAP	3-1
3.3	PDSP REGISTERS	3-2
3.3.1	Signature Register	3-2
3.3.2	A32 Base Address Register	3-3
3.3.3	Command/Status Register	3-3
3.3.4	DMA Interrupt Vector Register	3-5
3.3.5	DMA Primary & Backup Address Regs	3-5
3.3.6	DMA Primary & Backup Word Count Regs	3-6
3.4	VME DMA SYSTEM	3-6
3.5	OUTPUT DEVICE PROCESSING	3-7
3.6	OUTPUT MESSAGE FORMATS	3-8
3.6.1	Device Message Format Control	3-9
3.6.2	Header Message Word Selection	3-10
3.6.3	Device Control Words	3-11
SECTION 4	THEORY OF OPERATION	4-1
4.1	INTRODUCTION	4-1
4.1.1	Setup & Initialization	4-1
4.1.2	Input OP-code Word	4-1
4.1.3	Output OP-code Word	4-3
4.1.4	SHARC Algorithm Message	4-4
4.1.5	ID Word	4-4
4.1.6	Data Words	4-4
4.1.7	Input Data Conversion	4-5
4.1.8	CONDITIONAL ALGORITHM SEQUENCE	4-7
4.2	SHARC DSP	4-8
4.2.1	SHARC Output Format	4-8

4.2.2 Normal Message Outputs	4-9
4.2.3 Binary Time Message	4-9
4.2.4 Custom Algorithm Output Data	4-9
4.2.5 End Of Process (Flag 3)	4-9
SECTION 5 PDSP - SWITCH & JUMPER SETTINGS	5-1
5.1 DESCRIPTION	5-1
5.1.1 A16 Address Select	5-1
5.1.2 Factory Settings	5-1
5.1.3 U27 - DMA Address Mode	5-1
5.1.4 U27 - Interrupt Acknowledge Level	5-1
5.1.5 U27 - On Board Memory Size	5-1
5.1.6 JP1, JP3 - DMA Bus Grant & Request	5-1
5.1.7 JP2 - A-bus Request and Acknowledge	5-2
5.1.8 JP4 - Interrupt Request Level	5-2
5.1.9 JP5 - HOTLink<tm> Self Test Mode	5-2
5.1.10 JP7, JP8 - D-bus Priority Selection	5-2
5.1.11 JP9, JP10 - HOTLink<tm> Output Data Type	5-2
5.1.12 JP6 - On Board Clock Setting	5-2
5.1.13 JP11 - SHARC (DSP) JTAG connection	5-2
SECTION 6 DRAWINGS	6-1
6.1 INTRODUCTION TO THE DRAWINGS	6-1
6.1.1 Drawing System	6-1
6.1.2 Drawing Package Organization	6-1
6.1.3 Programmed Parts	6-2
SECTION 7 SCHEMATICS	7-1
7.1 INTRODUCTION	7-1
7.1.1 Schematic Conventions	7-1
7.1.2 Troubleshooting	7-1

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SECTION 1 INTRODUCTION

1.1 DESCRIPTION

The Model 505VA Programmable Data Stream Processor (PDSP) is a VME compatible, 6U card that performs algorithmic processing on raw telemetry data. The PDSP receives data from the Acroamatics Model 504VA Distribution & Host Interface card, accepting 32-bit ID, data, and instructions pertaining to what algorithm to perform. The PDSP performs over three hundred algorithms, including routines for integer-to-floating-point and floating-point-to-integer conversions. These algorithms include input and output data type conversion, data packing and compression, bit and limit checking, derived parameter calculation, 5th order polynomial conversion, and custom output formatting. The results are transmitted on the A-Bus to downstream devices for further data analysis.

1.1.1 Multiple Algorithms

You can perform multiple algorithms on a specific data sample, thereby processing data differently for various output devices. For example, you can process a datum with three algorithms as follows: First, *Scale And Send To DAC*; then do *Floating Compress*; finally, *Send Data To Host Interface*. The PDSP supports chained algorithms, so you can perform sequential operations - with each new algorithm using the results from the previous operation.

1.1.2 Derived Parameters

In addition, 32K of data memory provides the resources to calculate derived parameters based on the results of multiple arithmetic operations. The data memory stores temporary results, constants, lookup tables, as well as a current value table.

1.1.3 Output Formatting

Various algorithms process and format the data for transmission to devices such as digital-to-analog converters, discrete outputs, the Host DMA port, or the internal feedback port to the Distribution input. You can define the manner in which embedded time and data is formatted in the output stream to the Host interface. The Host DMA interface provides a method whereby formatted data may be routed to memory or networking devices residing on the VME Bus.

1.2 OPTIONS

There are two versions of the SHARC-based PDSP card:

Model	Description	Part Number
505VA-10	PDSP with 4096kB SRAM	6011505-10
505VA-11	PDSP with 1024kB SRAM	6011505-11

1.3 DOCUMENT CONVENTIONS

In this document register addresses and address offsets are hexadecimal numbers. Where it is necessary to refer to a hexadecimal number in the text, we use the C programming convention $0xNN$ to refer to hexadecimal number NN . Bits in a register are numbered in decimal. The term *Device n* refers to an address destination on the TDP system A-Bus. The A-bus is the output data bus, and has eight possible destination devices. Although we do not use all eight, those destinations we do use are dedicated to specific functions in the TDP system. The term *DIT* refers to a data message in the TDP system. It stands for “Data, ID, and Time”, the three components of a TDP data message. We can label a DIT by the value of its ID tag, for example “DIT 0xFFF1”, the DIT that conveys the once per millisecond value of a time message. Frequently we use a functional label instead, for example, “the MILLISECOND DIT”.

SPECIFICATIONS

MODEL VME 505VA - PROGRAMMABLE DATA STREAM PROCESSOR

FUNCTION	CHARACTERISTICS
INPUT BUS	interfaces data from eight possible 1602P PCM Frame Synchronizers, an IRIG port, a HOTLink™ port, and an optional 482P Analog to Digital port. Each datum is distributed as two 32-bit words; The first word is the identifier, containing time, status, and an ID tag, (up to 131,072 unique ID tags are supported), and the second word is the data.
DISTRIBUTION	Uses the ID tag value accompanying the datum to address a table in on-board memory defining the processing, routing, and post-processing destination of each input datum.
DEVICE BUS	Provides an interface to such devices as digital-to-analog outputs, digital discrete outputs, a local feedback to the Input Bus, serial HOTLink output, and a PCI-bus host DMA channel.
HOST INTERFACE	Provides controls for running the 1605P, as well as outputting and receiving data from the Device Bus. The PCI-bus host DMA channel provides a data path to and from host memory and devices
PROCESSING	An Analog Devices SHARC/(tm DSP performs simultaneous multiplier and ALU operations in a single clock cycle. The DSP is user-programmable with ADI software, which includes an optional C compiler.
INPUT DATA	Six 16-bit input types are supported: 2's complement, 1's complement, sign magnitude, offset binary, unsigned magnitude, and binary-coded-decimal. Three 32-bit types are supported: signed integers, IEEE, & MIL-Std floating point.
OUTPUT DATA	Five 16-bit input types are supported: 2's complement, 1's complement, sign magnitude, offset binary, and unsigned magnitude. Four 32-bit types are supported: signed & unsigned integers, IEEE, & MIL-Std floating point.
ALGORITHMS	Over 300 telemetry algorithms are provided, plus sequential algorithm chaining and user-defined expression processing. Algorithms include integer-to-floating point and floating point-to-integer conversions, limit and bit testing, data packing, linear data scaling, 5th order conversion, table lookup conversion, derived parameter calculation, and custom output formatting.
THROUGHPUT	Algorithm execution times range from a few hundred nanoseconds to several microseconds, with a maximum throughput for processed data of approximately 2.6 megasamples per second.
RECONSTRUCTOR	Operating as a data reconstructor or simulator, the 1605P accepts digital data from archival storage and reconstructs the original data stream, permitting reprocessing and analysis of stored data. The reconstructor may be set to output data at real-time, multiples of, or fractions of the real-time rate.
SERIALIZER	Accepts data from the PCI-bus via DMA or selected data from the input real-time stream and performs serialization and output at a selectable bit rate. This capability allows real-time retransmission of selected subsets of the input data.
POWER	+5VDC at 3.0A (excluding optional 482P)
ENVIRONMENTAL	Operating: 0 to +40°C; non-operating: -40 to +86°C
SHOCK	Operating: 6G; non-operating: 50G
VIBRATION	OPERATING: 0.5G, 5 to 2000 Hz; non-operating: 1.2G, 5 to 500 Hz

Specifications are subject to change without notice.

SECTION 2 INSTALLATION

2.1 GENERAL

This section contains installation information for the Acroamatics Model 505VA Programmable Data Stream Processor (PDSP). The card part number is either 6011505-10 or -11.

2.2 UNPACKING

Using proper ESD-protection procedures, open the cardboard shipping container and remove the card from the anti-static bag. Retain the container, anti-static bag, and foam packaging material for use if you must return the card.

2.3 FACTORY RETURN

When you return a card to the factory for repair or modification, include as much information as possible describing the failure mode or the modification~update you want.

Pack the card for shipment by wrapping it in the anti-static bag. Place the card into the shipping container, protecting it with the foam packing, and secure the container with reinforced tape. Provide the name and phone number of a technical contact we can talk to regarding the card.

Call Acroamatics at (805) 967-9909 to get a RMA number before returning any equipment to the factory, and include the RMA number in any correspondence or shipments to Acroamatics.

2.4 INSTALLING

The PDSP card mounts in a standard VMEbus chassis. Mounting dimensions are shown in the assembly Drawing in Section 6 of this manual. Slide the card into one of your system VME chassis slots and seat the card firmly by pressing against the ears. Make the front panel cable connections appropriate to your system. Remove the board by pulling firmly on the outside of the ears. For connector locations see Figure 2-1.

2.5 CONNECTORS

The following pages contain tables of information on all the connections into and out of the PDSP card.

TABLE 2-1. MATING CONNECTOR LIST FOR MODEL 505VA		
CONN.	FUNCTION	MATING CONNECTOR
P01	VMEbus	603-2-IEC-C096
P02	VMEbus	603-2-IEC-C096
J01	A OUT BUS	7964-6500EC
J02	HOTLink™ Data 1	SMB 903-285P-51S
J03	HOTLink™ Data 2	SMB 903-285P-51S

**TABLE 2-2. CONNECTOR LIST
MODEL 505VA BACKPLANE CONNECTOR P01-ROW-A**

NOTE: ALL (\$) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	4VMED00	Data Bus 00
02	4VMED01	Data Bus 01
03	4VMED02	Data Bus 02
04	4VMED03	Data Bus 03
05	4VMED04	Data Bus 04
06	4VMED05	Data Bus 05
07	4VMED06	Data Bus 06
08	4VMED07	Data Bus 07
09	GND	Ground
10	SYSCLK (\$)	System Clock
11	GND	Ground
12	9VMEDS1	Data Strobe 1
13	9VMEDS0	Data Strobe 0
14	9VMEWRT	Write
15	GND	Ground
16	9VMDACK	Data Transfer Acknowledge
17	GND	Ground
18	9VMASTB (\$)	Address Strobe
19	GND	Ground
20	9VMIACK	Interrupt Acknowledge
21	9VMIAIN	Interrupt Acknowledge IN
22	9VMIAOT	Interrupt Acknowledge OUT
23	4VMAM04	Address Modifier 4
24	4VMEA07	Address Bus 07
25	4VMEA06	Address Bus 06
26	4VMEA05	Address Bus 05
27	4VMEA04	Address Bus 04
28	4VMEA03	Address Bus 03
29	4VMEA02	Address Bus 02
30	4VMEA01	Address Bus 01
31	-12 VDC (\$)	-12 Volts DC
32	+5 VDC	+5 Volts DC

TABLE 2-3. CONNECTOR LIST MODEL 505VA BACKPLANE CONNECTOR P01-ROW-B		
NOTE: ALL (\$) SIGNALS UNUSED ON THIS CARD		
PIN	SIGNAL	FUNCTION
01	9VMBSBY (\$)	Bus Busy
02	9VMBCLR (\$)	Bus Clear
03	ACFAIL (\$)	AC Power Fail
04	9VMBGI0	Bus Grant 0 IN
05	9VMBGO0	Bus Grant 0 OUT
06	9VMBGI1	Bus Grant 1 IN
07	9VMBGO1	Bus Grant 1 OUT
08	9VMBGI2	Bus Grant 2 IN
09	9VMBGO2	Bus Grant 2 OUT
10	9VMBGI3	Bus Grant 3 IN
11	9VMBGO3	Bus Grant 3 OUT
12	9VMBRQ0 (\$)	Bus Request 0
13	9VMBRQ1 (\$)	Bus Request 1
14	9VMBRQ2 (\$)	Bus Request 2
15	9VMBRQ3 (\$)	Bus Request 3
16	4VMAM00	Address Modifier 0
17	4VMAM01	Address Modifier 1
18	4VMAM02	Address Modifier 2
19	4VMAM03	Address Modifier 3
20	GND	Ground
21	SERCLK (\$)	Serial Clock
22	SERDAT (\$)	Serial Data
23	GND	Ground
24	9VMIRQ7 (\$)	Interrupt Request 7
25	9VMIRQ6 (\$)	Interrupt Request 6
26	9VMIRQ5 (\$)	Interrupt Request 5
27	9VMIRQ4 (\$)	Interrupt Request 4
28	9VMIRQ3 (\$)	Interrupt Request 3
29	9VMIRQ2 (\$)	Interrupt Request 2
30	9VMIRQ1 (\$)	Interrupt Request 1
31	+5 VSTDBY (\$)	Stand-by +5 Volts DC
32	+5 VDC	+5 Volts DC

TABLE 2-4. CONNECTOR LIST
MODEL 505VA BACKPLANE CONNECTOR P01-ROW-C

NOTE: ALL (\$) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	4VMED08	Data Bus 08
02	4VMED09	Data Bus 09
03	4VMED10	Data Bus 10
04	4VMED11	Data Bus 11
05	4VMED12	Data Bus 12
06	4VMED13	Data Bus 13
07	4VMED14	Data Bus 14
08	4VMED15	Data Bus 15
09	GND	Ground
10	SYSFAIL (\$)	System Failure
11	9VMBERR (\$)	Bus Error
12	9VMPRST (\$)	System Reset
13	9VMELWD	Long Word
14	4VMAM05	Address Modifier 5
15	4VMEA23	Address Bus 23
16	4VMEA22	Address Bus 22
17	4VMEA21	Address Bus 21
18	4VMEA20	Address Bus 20
19	4VMEA19	Address Bus 19
20	4VMEA18	Address Bus 18
21	4VMEA17	Address Bus 17
22	4VMEA16	Address Bus 16
23	4VMEA15	Address Bus 15
24	4VMEA14	Address Bus 14
25	4VMEA13	Address Bus 13
26	4VMEA12	Address Bus 12
27	4VMEA11	Address Bus 11
28	4VMEA10	Address Bus 10
29	4VMEA09	Address Bus 09
30	4VMEA08	Address Bus 08
31	+12 VDC (\$)	+12 Volts DC
32	+5 VDC	+5 Volts DC

TABLE 2-5. CONNECTOR LIST
MODEL 505VA BACKPLANE CONNECTOR P02-ROW-A

PIN	SIGNAL	FUNCTION
01	4DRYOP4	ACRO PDSP4 Bus Ready For Opcode
02	4DRYOP3	ACRO PDSP3 Bus Ready For Opcode
03	4DRYOP2	ACRO PDSP2 Bus Ready For Opcode
04	4DRYOP1	ACRO PDSP1 Bus Ready For Opcode
05	9DCMRP4	ACRO PDSP4 Distribution Bus Request
06	9DCMRP3	ACRO PDSP3 Distribution Bus Request
07	9DCMRP2	ACRO PDSP2 Distribution Bus Request
08	9DCMRP1	ACRO PDSP1 Distribution Bus Request
09	9DFORCE	ACRO Data Force Flag
10	4DCMFCF	ACRO PDSP Finished With Data
11	9RFADSL	ACRO Distribution Reference Address Select
12	GND	ACRO Ground
13	9DCMWRT	ACRO Distribution Memory Write
14	4DBUS00	ACRO Distribution Data Bus 00
15	4DBUS01	ACRO Distribution Data Bus 01
16	4DBUS02	ACRO Distribution Data Bus 02
17	4DBUS03	ACRO Distribution Data Bus 03
18	4DBUS04	ACRO Distribution Data Bus 04
19	4DBUS05	ACRO Distribution Data Bus 05
20	4DBUS06	ACRO Distribution Data Bus 06
21	4DBUS07	ACRO Distribution Data Bus 07
22	GND	ACRO Ground
23	4DBUS23	ACRO Distribution Data Bus 23
24	4DBUS22	ACRO Distribution Data Bus 22
25	4DBUS21	ACRO Distribution Data Bus 21
26	4DBUS20	ACRO Distribution Data Bus 20
27	4DBUS19	ACRO Distribution Data Bus 19
28	4DBUS18	ACRO Distribution Data Bus 18
29	4DBUS17	ACRO Distribution Data Bus 17
30	4DBUS16	ACRO Distribution Data Bus 16
31	GND	ACRO Ground
32	9SRSTP1	ACRO PDSP Reset

TABLE 2-6. CONNECTOR LIST
MODEL 505VA BACKPLANE CONNECTOR P02-ROW-B

NOTE: ALL (\$) SIGNALS UNUSED ON THIS CARD

PIN	SIGNAL	FUNCTION
01	+5 VDC	+5 Volts DC
02	GND (\$)	Ground
03	RESERVED (\$)	
04	4VMEA24	Address Bus 24
05	4VMEA25	Address Bus 25
06	4VMEA26	Address Bus 26
07	4VMEA27	Address Bus 27
08	4VMEA28	Address Bus 28
09	4VMEA29	Address Bus 29
10	4VMEA30	Address Bus 30
11	4VMEA31	Address Bus 31
12	GND	Ground
13	+5 VDC	+5 Volts DC
14	4VMED16	Data Bus 16
15	4VMED17	Data Bus 17
16	4VMED18	Data Bus 18
17	4VMED19	Data Bus 19
18	4VMED20	Data Bus 20
19	4VMED21	Data Bus 21
20	4VMED22	Data Bus 22
21	4VMED23	Data Bus 23
22	GND	Ground
23	4VMED24	Data Bus 24
24	4VMED25	Data Bus 25
25	4VMED26	Data Bus 26
26	4VMED27	Data Bus 27
27	4VMED28	Data Bus 28
28	4VMED29	Data Bus 29
29	4VMED30	Data Bus 30
30	4VMED31	Data Bus 31
31	GND	Ground
32	+5 VDC	+5 Volts DC

TABLE 2-7. CONNECTOR LIST		
MODEL 505VA BACKPLANE CONNECTOR P02-ROW-C		
PIN	SIGNAL	FUNCTION
01	9PILCK4	ACRO PDSP4 Opcode Clock
02	9PILCK3	ACRO PDSP3 Opcode Clock
03	9PILCK2	ACRO PDSP2 Opcode Clock
04	9PILCK1	ACRO PDSP1 Opcode Clock
05	9DCMAK4	ACRO PDSP4 Distribution Bus Acknowledge
06	9DCMAK3	ACRO PDSP3 Distribution Bus Acknowledge
07	9DCMAK2	ACRO PDSP2 Distribution Bus Acknowledge
08	9DCMAK1	ACRO PDSP1 Distribution Bus Acknowledge
09	9RSTFFL	ACRO Data Force Reset
10	9TSTMOD	ACRO PDSP Test Mode
11		Not Used
12	GND	ACRO Ground
13	9DSEQ02	ACRO ID-Data Output Enable
14	4DBUS08	ACRO Distribution Data Bus 08
15	4DBUS09	ACRO Distribution Data Bus 09
16	4DBUS10	ACRO Distribution Data Bus 10
17	4DBUS11	ACRO Distribution Data Bus 11
18	4DBUS12	ACRO Distribution Data Bus 12
19	4DBUS13	ACRO Distribution Data Bus 13
20	4DBUS14	ACRO Distribution Data Bus 14
21	4DBUS15	ACRO Distribution Data Bus 15
22	GND	ACRO Ground
23	4DBUS31	ACRO Distribution Data Bus 31
24	4DBUS30	ACRO Distribution Data Bus 30
25	4DBUS29	ACRO Distribution Data Bus 29
26	4DBUS28	ACRO Distribution Data Bus 28
27	4DBUS27	ACRO Distribution Data Bus 27
28	4DBUS26	ACRO Distribution Data Bus 26
29	4DBUS25	ACRO Distribution Data Bus 25
30	4DBUS24	ACRO Distribution Data Bus 24
31	GND	ACRO Ground
32	9SCLKP1	ACRO PDSP Clock

TABLE 2-8. CONNECTOR LIST
MODEL 505VA FRONT PANEL CONNECTOR J01

PIN	SIGNAL	FUNCTION
01		Not Used
02	9AWORD1	A Bus Last Word Flag
03	4SFLAG1	A Bus Last Transfer Flag
04	4APORT1	A Bus Port Select 1
05	GND	Ground
06	4APORT0	A Bus Port Select 0
07	4ADEST2	A Bus Destination Select 2
08	4ADEST1	A Bus Destination Select 1
09	4ADEST0	A Bus Destination Select 0
10	4AOUT15	A Bus 15
11	4AOUT14	A Bus 14
12	GND	Ground
13	4AOUT13	A Bus 13
14	4AOUT12	A Bus 12
15	4AOUT11	A Bus 11
16	4AOUT10	A Bus 10
17	GND	Ground
18	4AOUT09	A Bus 09
19	4AOUT08	A Bus 08
20	4AOUT07	A Bus 07
21	4AOUT06	A Bus 06
22	4AOUT05	A Bus 05
23	4AOUT04	A Bus 04
24	GND	Ground
25	4AOUT03	A Bus 03
26	4AOUT02	A Bus 02
27	4AOUT01	A Bus 01
28	4AOUT00	A Bus 00
29	GND	Ground
30	9AOACK0	A Bus Acknowledge 0
31	9AOREQ0	A Bus Request 0
32	GND	Ground
33	9AOACK1	A Bus Acknowledge 1
34	9AOREQ1	A Bus Request 1
35	GND	Ground
36	9AOACK2	A Bus Acknowledge 2
37	9AOREQ2	A Bus Request 2
38	GND	Ground
39	9AOACK3	A Bus Acknowledge 3
40	9AOREQ3	A Bus Request 3

TABLE 2-8. (continued) CONNECTOR LIST MODEL 505VA FRONT PANEL CONNECTOR J01		
PIN	SIGNAL	FUNCTION
41	GND	Ground
42		Not Used
43	9AOREST	A Bus Reset
44	GND	Ground
45	4AOUT31	A Bus 31
46	4AOUT30	A Bus 30
47	4AOUT29	A Bus 29
48	4AOUT28	A Bus 28
49	4AOUT27	A Bus 27
50	4AOUT26	A Bus 26
51	4AOUT25	A Bus 25
52	4AOUT24	A Bus 24
53	4AOUT23	A Bus 23
54	4AOUT22	A Bus 22
55	4AOUT21	A Bus 21
56	4AOUT20	A Bus 20
57	4AOUT19	A Bus 19
58	4AOUT18	A Bus 18
59	GND	Ground
60		Not Used
61	9ALWORD	A Bus Long Word
62	GND	Ground
63	4AOUT17	A Bus 17
64	4AOUT16	A Bus 16

TABLE 2-9. CONNECTOR LIST MODEL 505VA FRONT PANEL CONNECTOR J02		
PIN	SIGNAL	FUNCTION
01	4AOUTA	HOTLink™ Output 1 +
02	9AOUTA	HOTLink™ Output 1 -

TABLE 2-10. CONNECTOR LIST MODEL 505VA FRONT PANEL CONNECTOR J03		
PIN	SIGNAL	FUNCTION
01	4AOUTB	HOTLink™ Output 2 +
02	9AOUTB	HOTLink™ Output 2 -

SECTION 3 OPERATION

3.1 GENERAL

The VME Host computer configures the Model 505VA PDSP card by way of an interface to twenty separate registers and 3M Bytes of on-card program memory. The registers map into A16 memory space on switch-selected 64 byte boundaries. One of these is the *SignatureRegister*, which the software reads to determine the options on your PDSP card. Another register contains a *memory offset* to address a specific 4 MByte page in A32-D32 memory space on the VMEBus, where the host can access the 3 MBytes of program memory.

3.2 PDSP MEMORY MAP

We have provided system software, such as the Acroamatics compiler, with access to the SHARC I/O registers and program/data memory, a Current Value Table in SRAM, and sixteen A-Bus Output Format Description registers by mapping these functions into the VME memory as shown in TABLE 3-1.

The first 1 MByte partition is the address space of the Analog Devices SHARC/(tm DSP. The first 512kB of this block contains only 256 I/O registers. These registers configure the SHARC™ and then generate a software interrupt to the SHARC processor (after the program has been downloaded) to start program execution. The second 512kB is partitioned by the SHARC software into 48-bit *instruction* and 32-bit *data* memories. A detailed explanation of these functions appears in the Analog Devices ADSP-2106X SHARC Users Manual.

SHARC 1 MByte	IOP Registers	00000000
	Memory	00080000
A-BUS 1 MByte	A-BUS Format Control Registers	00100000
	not used	100044
SRAM 4 MByte	1 MByte SRAM	00200000
	1 MByte or 3 MByte SRAM Option	00300000
		00400000
		or
		00600000

TABLE 3-1. VME Address Map for A32/D32 Instructions

The second 1 MByte of address space contains sixteen 32-bit setup registers that configure the output processor. The A-Bus output processor formats and transfers data to ten output channels. Four channels are fixed format, while the other six have user programmable formats. The setup is downloaded as 16 32-bit words. The contents of the format control word are described later in this document. The 17th 32-bit address in this block (100040) reads data from the SHARC data bus during test mode. This allows you to monitor (for test purposes) data transfers from the distribution input processor, as well as transfers from the SHARC DSP to the output section. The final 1 MByte of address space initializes and accesses the SRAM that provides a current value table, as well as storing constants and temporary values for some algorithms. The basic card provides 128k 32-bit words, while the expanded version provides 256k.

3.3 PDSP REGISTERS

The PDSP registers contain *command* and *status* information. Register locations are memory-mapped in the A16 Utility Address Space on switch-selectable 64-byte boundaries. You access the registers through nonprivileged or supervisory A16/D16 memory instructions. Allocation of the A16 utility space appears in TABLE 3-2 below. Brief descriptions of the registers follow the table.

A16 Utility Registers		
Addr	Function	Mode
0	Signature	Read/Write
2	A32 Base Address	Read/Write
4	Command/Status	Read/Write
6	DMA Interrupt Vector	Read/Write
8	DMA Primary Address (A31-A16)	Read/Write
A	DMA Primary Address (A15-A2)	Read/Write
C	DMA Backup Address (A31-A16)	Write Only
E	DMA Backup Address (A15-A2)	Write Only
10	DMA Primary Word Count	Read/Write
12	DMA Backup Word Count	Write Only
14-3F	Reserved	

TABLE 3-2. Distribution & Host Interface A16 Registers

3.3.1 Signature Register

The Signature Register identifies the installed 505VA card for system configuration purposes, and reading this register will return a value of $x505_{hex}$ with the value of x shown in TABLE 3-3. Reading a value of 0505 identifies the original, non-dash-numbered PDSP (Programmable Data Stream Processor) card, described in *Technical Manual - 505V Programmable Data Stream Processor*, Acroamatics Document Number 6000245. For non-zero values of x, the value of x defines the dash numbered options available on the 505VA-10 and -11, as shown in TABLE 3-3.

Signature Register			
Addr	Signature	Description	Mode
0	0505	Old 505V	Read
0	4505	505VA-11 PDSP - 1024kB SRAM	Read
0	5505	505VA-10 PDSP - 4096kB SRAM	Read

TABLE 3-3. Signature Register

3.3.2 A32 Base Address Register

The Base Address Register establishes the A32 block address for the PDSP functions that are memory mapped. The card requires a 4 MByte address block and therefore uses the 10 MSBs of this register to form the 10 MSBs of all A32 address accesses. The two LSBs of this register control special features when making DMA transfers. These features maximize the DMA transfer rate by hogging the bus, but allow other DMA channels on the same bus arbitration level to have access to the bus without undue bus latency.

Bit 0 ON enables the DMA arbitration to be a *FAIR MODE* requester. When set, the arbitration logic monitors the bus request line after it completes a DMA transfer, and will not reacquire bus control until all of the DMA users on that bus level have had access to the bus. When set to 0, the DMA will reacquire the channel as quickly as possible.

Bit 1 ON causes the DMA channel to relinquish bus control after 64 transfers even though there is more data to transfer. When set to 0, the DMA will retain bus control until it has transferred all available data.

3.3.3 Command/Status Register

The Command/Status Register provides control for the Host DMA interface and 505V PDSP cards. TABLE 3-4 lists the command and status bits of the register.

COMMAND/STATUS REGISTER		
Bit	Function	Mode
15	Test Data Ready	Read
15	Test Mode Select	Write
14	A-Bus FIFO empty	Read
13	DMA FIFO empty	Read
12	Auto Link Enable	Read/Write
11	Host DMA Interface Enable	Read/Write
10	Host DMA Interface Reset	Write Only
9	DMA Backup Address Loaded Status	Read Only
8	DMA Primary Address Loaded Status	Read
8	Enables the writing of Bits 12-11	Write
7	DMA FIFO Full Interrupt Status	Read
7	Enables the writing of Bits 0-3	Write
6	not used	
6	Clear Interrupt Status Bits 4-7	Write
5	DMA End of Process Interrupt Status	Read Only
4	DMA Terminal Count Interrupt Status	Read Only
3	DMA FIFO Full Interrupt Enable	Read/Write
2	not used	
1	DMA End of Process Interrupt Enable	Read/Write
0	DMA Terminal Count Interrupt Enable	Read/Write

TABLE 3-4. Command/Status Register

Bit 15 is set to **1** to select test mode.

Bit 15 - is set to **1** when test data is available.

Bit 14 - is set to **1** when the A-Bus FIFO is empty.

Bit 13 - is set to **1** when the DMA FIFO is empty.

Bit 12 - is set to **1** for *DMA autolink* which automatically loads the address and word count from the backup registers each time terminal count is reached. Bit 8 must be set to **1** to write this bit.

Bit 11 - enables the Host DMA channel to accept data from the output device processor. Bit 8 must be set to **1** to write this bit.

Bit 10 - clears the DMA data FIFO and the Primary and Backup Address Loaded status.

Bit 9 - indicates the Backup Address was loaded into the DMA address generator.

Reading bit 8 high indicates that there is a primary DMA Address loaded into the address generator. Writing bit 8 high enables the writing of the register bits 12 and 11.

Bits 7 through 4 - are Interrupt Status - used for polling the source of an interrupt. The bits remain set until cleared by writing bit 6 high. If an interrupt occurs before the Interrupt Status bits are cleared, the second interrupt and its status bits are queued until the current interrupt status is cleared. The interrupt status bits are masked by the corresponding interrupt enables, bits 3

through 0.

The reading of bit 7 high indicates the interrupt was caused by the DMA data FIFO becoming full. Writing bit 7 high enables the writing of the register bits 3 through 0 of the register.

Writing bit 6 high clears the current interrupt status.

Bit 5 - indicates an End of Process signal from the DMA interface was detected, signifying the end of a data buffer transmission.

Bit 4 - indicates the host DMA word counter reached terminal count.

Bits 3 through 0 are the enables for the corresponding interrupt sources. Bit 7 of the Command/Status Register must be set to program bits 3 through 0.

Bit 3 - enables the DMA FIFO full interrupt.

Bit 2 - is not used.

Bit 1 - enables an interrupt when a DMA *End of Process* signal is detected. When EOP mode is enabled, an external EOP will generate an interrupt and the hardware will save the current value of the Primary Word Count register until the register is read by the interrupt program. This allows the program to determine the size of variable length DMA records.

Bit 0 - enables an interrupt when DMA word counter reaches terminal count.

3.3.4 DMA Interrupt Vector Register

The DMA Interrupt Vector Register establishes a 16-bit address used for vectoring to the interrupt service routine.

3.3.5 DMA Primary & Backup Address Regs

The DMA Primary and Backup Address Registers are initialized with the starting A32 address for DMA block transfers. Loading the least significant portion of the Primary Address Register initiates DMA transfers. Upon each DMA transfer, the address generator auto-increments until either an End of Process signal is detected or the terminal count is reached. Once the DMA transfer completes, the address generator and word counter are reinitialized from the Backup Address Register and the Backup Word Count Register.

The Backup Address Register is initialized to the starting address of the next DMA buffer. The contents of the Backup Address register are automatically loaded into the address generator each time the word count reaches zero or an EOP is detected. When the Backup Address Register is initialized, the Backup Address Loaded status asserts high. It remains asserted until the DMA block transfer completes. The Backup Address Register must be reloaded each time for multiple data buffers.

3.3.6 DMA Primary & Backup Word Count Regs

The Primary and Backup Word Count Registers are programmed with a 16-bit value corresponding to the number of words per DMA block transfer. The DMA word counter is preset to the value stored in the register, and then decrements upon each DMA transfer. When the count reaches zero, a terminal count interrupt is generated, and the word counter is reinitialized to the contents of the Backup Count Register.

The primary word counter is a read/write register. The read operation has a special function when the EOP interrupt bit is set ON in the Distribution Command/Status Register (bit 1 of address 4). An external EOP generates an interrupt when the EOP mode is enabled, and the contents of the primary word count register will be saved (in a separate register) until the register is read by the interrupt service program. This allows the program to determine the size of variable length DMA records.

3.4 VME DMA SYSTEM

The DMA system on the 505VA card is a one way transfer of data from the distribution input logic, through the SHARC DSP to the output device processor and the formatted data stream is FIFO'ed and transferred to the VME memory; it does not transfer data from the VME memory.

A 32-bit counter register called the *Primary Address Register* always contains the address of the next location to be accessed in VME memory. Two 16-bit transfers to the Primary Address Register (at address offsets 08 and 0A) load the starting A32 address for a block transfer. The Primary Address Register indicates it is loaded (DMA Status Register bit 8 reads as 1) upon loading the least significant 16 bits into address 0A.

A 16-bit *Primary Word Count* register holds the number of 32-bit words awaiting transfer from VME memory. (load this register with zero for a transfer count of 65536). When the Primary Address Register has loaded status and the DMA Interface is enabled, the DMA transfers initiate. You should load the Primary Word Count register previous to this. The 32-bit *Backup Address* register (formed by addresses 0C and 0E) holds the starting A32 address for the *next* block transfer that will occur after the *primary* transfer is complete. The 16-bit *Backup Count* register (address 12) contains the transfer length of that next block transfer.

the Primary Address register auto-increments with each DMA transfer. The Primary Word Counter auto-decrements until it reaches zero, signifying completion of the DMA transfer. If the Backup Address register is loaded, it's contents are transferred to the Primary Address Register while, in a similar fashion, the Backup Count register contents are transferred to the Primary Count Register and the DMA transfer continues. When the Backup Address register is empty the DMA transfer stops. In either case, an interrupt occurs if the DMA Terminal Count Interrupt is enabled.

The Backup Address register becomes loaded (DMA Status Register bit 9 reads as 1) when you load the least significant half (address 0E). A reasonable loading order is Backup Count, Backup Address MSH, and then Backup Address LSH. If the Primary Address is not loaded, the DMA is idle and the Backup Registers transfer immediately to the Primary Registers. If the Primary Address is loaded, the Backup Address retains *loaded* status until the DMA block transfer completes and the Backup Registers transfer to the Primary Registers. You then

reload the Backup Registers. Thus you can consider the Primary and Backup registers a two location queue. You never have to load the Primary registers directly when you are performing double-buffered data transfers. For single buffered operation it is more convenient to use the Primary registers.

When *Autolink* is enabled (command register bit 12 set to **1**), the address register and word counter are reloaded from the last value in the backup registers without requiring the host to reload these registers. Each time *terminal count* is reached the DMA will start a new record with the same size and same address as the previous record. This feature allows a high speed device to extract and record data without host intervention.

3.5 OUTPUT DEVICE PROCESSING

The output processing section receives data, ID tags, fine time (microseconds) and time of day in either binary or BCD format from the distribution input and/or SHARC processor. Each data sample contains an output data type field that defines a 16 or 32 bit sample and a destination field that defines one of ten destinations. Some destinations have two *port bits* that allow that device to support up to four output ports. The output device field specifies the message destinations as shown in the following table.

OUTPUT DESTINATIONS				
Dest.	Description	Word Format		
		Word Size	DIT	Data Only
0	Digital Output 0	16/32	32/64	32
1	Digital Output 1	16/32	32/64	32
2	Digital Output 2	16/32	32/64	32
3	Digital Output 3	16/32	32/64	32
4	Feedback Port	16/32	64*	no
5	Multifunction (dedicated)	16/32	32*	no
6	Host Input Register	16/32	32*	no
7	DAC Bus	16/32	32*	no
8	High Speed Serial Output	32	32/64	32
9	DMA Channel	32	32/64	32

**these devices have fixed output formats*

TABLE 3-5. Output Destinations

The first four outputs listed above are general purpose A-Bus destinations that may support the two *port lines* to further define the final message destination. The A-Bus is a general purpose output bus that supports either 16 or 32 bit transfers.

All of the hardware connected to the A-Bus currently accepts 16 bit input words. As these functions are re-mechanized, the bus width will be extended to 32 bits to increase the output bandwidth.

Devices *Four to Seven* are predefined hardware that receives fixed format messages to perform predefined functions. Several different output cards use devices *Zero to Three*, with The DMA channel on the 504VA distribution card the

most commonly used. The Feedback Port (Device 4), Host Input Register (Device 6), a parallel to serial converter and an illegal opcode register (Device 5) are also on the Distribution card. Messages to the DAC Bus (Device 7) are connected directly to the 506V Digital to Analog Converter cards. There are two output devices, supported by hardware on the 505VA card, and therefore do not require connection to the A-Bus. The first (Device 8) is a high speed parallel to serial converter that accepts a 32 bit word and transmits it as a 330 Megabit serial stream. The second (Device 9) is the internal DMA channel which accepts 32 bit words and transfers them to an address on the VME bus.

3.6 OUTPUT MESSAGE FORMATS

You can select any of fifteen different programmed output formats for the data stream going to host computer by way of general purpose devices on the A-Bus, by a high rate serial channel, or a programmable DMA. There are also four hardware output formats. Which one you choose depends upon how you intend to process the data, what the input data rate is, and how fast your host computer can save the data to its storage medium.

The TDP can create block formatted data records and then send a signal to your host interface to mark the last word transferred in each data block. If your host interface can respond to this signal (the PDSP DMA can), you can use it to synchronize block transfers. The blocked data records may be preceded by a programmable block header, that may contain a TIME stamp, up to four fixed data values, the block length value, and the contents of a block counter. You can program the order in which the block header is constructed.

If you use your host computer to record the data, you must understand what your computers limitations are. Computer sales literature often leads you to unrealistic expectations because it quotes data processing rates that are the highest rates achievable by the hardware. Disk transfer rates are often the instantaneous rates that can be achieved to the disk cache buffer, not the sustained transfer rates that can be achieved considering the speed penalties imposed by rotational latency and layer upon layer of operating system software overhead.

The TDP's variety of output formats can help you with the compromises you may have to make in order to successfully record data on your host computer. If you have to choose to discard whole blocks of data, recording only sampled intervals, the time header output formats let you easily determine what intervals have been recorded. If you must give up ID tags in order to get your data recorded, you can choose formats that transmit data-only to the host. If you have low rate data and plenty of host transfer bandwidth and data storage space, you can choose the luxury of floating point output format with microsecond time tags on every data sample.

The PDSP Output Algorithms are user-selectable by program commands, and the default Output Algorithms are set by the assigned value of an environment variable or by including commands in your setup program. Different default output algorithms may be set for each of the output devices. If you want to override any of the channel default selections, program the channels with the software commands described in Section 4.3.2 of *Programming Manual for the VMEbus Telemetry Data Processors Floating Point Data Distribution System*, Acroamatics Document Number 6000265.

Although the A-Bus data path is normally sixteen bits wide, transfers on the VME bus by way of the DMA are made into 32-bit words by the interface. The sixteen bit transfers accumulate in a register file and the VME bus transfer occurs when a 32-bit word has been assembled. Synchronizing signals that the generates assure that these messages are always assembled in the correct order. The data messages are described below as 32-bit long words as you would see them in VME memory. Keep in mind that if you manipulate these using your host computer, different manufacturers have different addressing conventions for 16-bit and 8-bit fields of the 32-bit word. In the discussion that follows, the unqualified word *word* means a 32-bit data word.

3.6.1 Device Message Format Control

Six of the ten output devices have user selectable output formats. Each output format is defined to the compiler, which prepares and downloads sixteen 32-bit words in the A-bus format control portion of the memory mapped setup. The table below defines the contents of the setup message that controls each devices output format and, if required, the header message content.

DEVICE MESSAGE FORMAT CONTROL WORDS		
Byte	Description	
Address	31 ←	→ 0
00	Device 1 Control	Device 0 Control
04	Device 3 Control	Device 2 Control
08	Device 9 Control	Device 8 Control
0C	Fixed Word 2	Fixed Word 1
10	Fixed Word 4	Fixed Word 3
14	Fixed Word 6	Fixed Word 5
18	A-bus Size	Time Word ID
1C	Device 1 Block Length	Device 0 Block Length
20	Device 3 Block Length	Device 2 Block Length
24	Device 9 Block Length	Device 8 Block Length
28	Device 0 Header Control	Device 0 Header Control
2C	Device 1 Header Control	Device 1 Header Control
30	Device 2 Header Control	Device 2 Header Control
34	Device 3 Header Control	Device 3 Header Control
38	Device 8 Header Control	Device 8 Header Control
3C	Device 9 Header Control	Device 9 Header Control

TABLE 3-6. Device message Format Control Words

Bytes 0-11 - provide six 16-bit control words that allow you to programmably control the type of message and the format of the output stream for each of the six output devices that provide programmable formats. Devices 4, 5, 6, & 7 are fixed format. The A-bus size for these devices is selected in register 18. The contents of the device control word are shown in TABLE 3-10.

Bytes 0C-17 - provide six 16-bit fixed data words. You can insert these words at programmable locations within the record header message.

Bytes 18-1B - The 17 LSBs of this word provide the ID tag for the one millisecond time word. This specially formatted BCD Time of Day message is captured by the device output control logic and may be included in the block header message. Bits 17-20 are individual device enables that specify the A-bus size (1 = 32 bit, 0 = 16 bit) for the four fixed format devices. Bit 17 determines device 4 bus size and bit 20 determines Device 7 bus size.

Bytes 1C-27 - are six 16 bit words that provide the block length (in bytes) for devices that are programmed to divide the stream into fixed length records.

Bytes 28-3F - are six 32 bit header control words that arrange the header information in the header portion of each new record. The word is divided into eight 4 bit fields. These fields select header words that are included in the header message and the order in which they are included. Bits 0-3 control the first header word by their values. The values and their header word selection is shown in TABLE 3-7. The fields are scanned from LSB to MSB and the header message is terminated when a zero value is reached or automatically at the end of the eighth header word.

3.6.2 Header Message Word Selection

Blocked formats may sometimes be preceded by a header message that can contain up to five components. These components are selected by the appropriate device header control word that determines the message content and sequence. The words are selected by eight 4-bit fields that specify which word will be output at a specific header sequence. The header message is terminated when the word selection field is zero, or at the completion of the fifth message. The time message is a 64 bit word that can be binary or BCD as shown in TABLES 3-8 and 3-9. The remaining messages are all 16 bit words.

HEADER MESSAGE WORD SELECTIONS	
Field	Description
0	End of Message
1	Time (64 bits)
2	Block Length
3	Block Number
4	Fixed Word 1
5	Fixed Word 2
6	Fixed Word 3
7	Fixed Word 4
8	Fixed Word 5
9	Fixed Word 6

TABLE 3-7. Header Message Word Selections

BCD TIME MESSAGE FORMATS								
63 ←		Bit						→ 32
100 μ sec*	10 μ sec*	1 μ sec*	100 D	10 D	Days	10 H	Hours	
31 ←		Bit						→ 0
10 M	Mins	10 Sec	Seconds	100 ms	10 ms	ms	.1 ms	
<i>* μseconds are optional</i>								

TABLE 3-8. BCD Time Message Format

BINARY TIME MESSAGE FORMAT		
63 ←		bit → 32
BCD μ seconds*	not used	Binary Day of Year
Binary Milliseconds of Day		
31 ←		bit → 0
<i>* μseconds are optional</i>		

TABLE 3-9. Binary Time Message Format

3.6.3 Device Control Words

The setup message contains ten 16 bit words that control message formation for each output device. The words define the message type, device bus size, frame synchronous message, binary or BCD time, block length counter controls, block size controls, block format enable, EOP enable and record fill control.

DEVICE CONTROL WORD CONTENTS	
Bit	Description
0	Message Type LSB
1	Message Type -
2	Message Type MSB
3	not used
4	Device Size = 32 bits
5	not used
6	Binary Time Enable
7	Include μ seconds
8 α	Blocked Format Enable
9	not used
10	not used
11	Block Count Enable
12 β	EOP Enable
13	not used
14	not used
15	Device 8 sends command 1 at start of frame
	α - Device 8 will send command 0 at start of block β - Device 8 will send command 2 at EOP

TABLE 3-10. Device Control Word Contents

Bits 0-2 specify the type of output format for each device. The bit coding is shown in TABLE 3-11.

Bit 3 - in the device control word is not used.

Bit 4 - selects the output device register size. Devices on the A-Bus are normally 16 bits. However, as the hardware is remechanized, the register width will be increased to 32 bits to increase transfer bandwidth. Devices 8 and 9 are 32 bits wide. Bit 4 is set to **1** to select 32 bits or set to **0** to select 16 bit device bus widths.

Bit 5 - Start of Message Enable. This bit is set to **1** to require the output message to start at a selected word in the input stream (such as a minor or major frame word). The start of frame flag is generated by the DSP in response to specific algorithms.

Bit 6 - is set to **1** to enable binary time to be used when time is included in the block header message.

Bit 7 - is set to **1** to include μ seconds in the time header message.

Bit 8 - is set to **1** to enable blocked format. The block length is specified by the block length setup register, which contains the number of 8-bit messages (excluding the header) for that device.

Bit 9 - is set to **1** to enable you to fill variable length records to form fixed length blocks. When this feature is enabled the fill length counter is written as the last word of each block. When EOP is received with the normal last word of a block, the fill counter will be at zero. When the received block length is less than the programmed length, the fill counter contains the number of fill data bytes used

to complete the block.

Bit 10 - is set to **1** when the fill counter word, which is written at the end of block, is a 32 bit word. The bit is set to **0** for a 16 bit word.

Bit 11 - is set to **1** to enable the block counter when the block count is to be included in the block header message.

Bit 12 - is set to **1** to enable the EOP signal in conjunction with blocked message formats.

For blocked output formats, the output hardware counts a fixed number of words, then sends the last word of each block with a signal called EOP (End Of Process). The interface uses this signal to terminate the current block transfer and begin a new block. The TDP does not normally set this signal for unblocked output formats but the algorithms **PLW**, **PLWT**, and **QEOF** will cause all output subroutines to transmit the last word with EOP. These algorithms also cause the output subroutines for blocked output formats to reset their block length counters, and cause subroutines that do a time header to output a new header with the next word transmitted.

Bit 13 - is set to **1** to allow the last output block to be completed with fill data. When the output device is disabled. Bit 13 set to **0** causes the hardware to attempt to complete the current buffer with incoming data and then disable the output device.

Bits 14 & 15 - are not used.

DEVICE OUTPUT FORMATS			
Bit			Description
2	1	0	
0	0	0	12 bits ID, 4 fine time, 16 data bits
0	0	1	13 bits ID, 2 status, 1 time tick, 16 data bits
0	1	0	16 bits ID, 16 data bits
0	1	1	17 bits ID, 2 status, 12 fine time, 32 data bits
1	0	0	no ID, 32 data bits
1	0	1	not used
1	1	0	not used
1	1	1	not used

TABLE 3-11. Device Output Formats

The first three message types whose descriptions follow pack the DIT into a single 32-bit word. Since the DIT as received on the TDP input is a 64-bit message, there is plainly a compromise: we truncate the ID tags and limit the data to SHORT (16-bit). If you have mostly SHORT data and a moderate number of unique IDs, this compromise doubles your bandwidth and halves your storage requirements. To circumvent this limitation when you process LONG data words, the PDSP output subroutines that output only SHORT data automatically convert a LONG data word into two DITs, setting the LSB of the ID tag field of the second DIT to **1**. The most significant sixteen bits of the data appear in the first DIT, the least significant in the second DIT. All of this means that if you output a LONG data word with an even ID tag, you will see two DITs in the output stream, the first with the specified ID tag, the second with the specified tag plus **1**. If you output a LONG data word with an odd ID tag, you will see two

DITs in the output stream, both with the specified ID tag.

All output formats generate a stream of DITs for formats 0 through 3. and packed data words for format 4. You can select the output as frame synchronous by setting bit five to 1 which requires the stream for that device to start with a word that carries a *start of frame* flag you program. You can block the stream into records by enabling the block length counter. You program the block length from one to 65,535 32-bit words and you can also insert a programmable header message at the beginning of each block. When bit 12 is set to 1 and the output format is blocked, the last word of each message is sent with a signal called **EOP** (End of Process). The external interface can use this signal to terminate the current block transfer and begin a new block. EOP is normally used to synchronize the output block to input frames.

FORMAT 0:

Data and ID tag with Fine Time

The DIT consists of 32-bit word: The most significant four bits contain a time tag representing 0.1 milliseconds. The next twelve bits are the ID tag, which means that the maximum ID representable is 4095. The MSBs of the ID as generated by an input device are deleted, which means TDP reserved IDs in the range 8100-8191 are output as 4004-4095. The time tag field tags the datum with the tenth of a millisecond. Every millisecond, this field will be 'F' (all ones) - this state is called the "tick". The advantage of this tick field is that it is quickly and easily detected by software or hardware that processes the data after it leaves the TDP. The word carrying the tick is the first word output to the specified device following the ID tag for the millisecond DIT is specified in the header message format control setup words. The data part of the message occupies the sixteen LSBs.

The schematic of the data message is:



FORMAT 1:

Data and ID with Tick and Status Bits

The DIT consists of a 32-bit word. The most significant bit is a parity error bit, the next is a not-in-lock bit, and the next is a "time tick" bit representing one millisecond. The ID consists of the next thirteen bits. The 16 LSBs are again the 16-bits of data. As described for the data format with fine-time, above, the first word output to the specified device will generate the tick. If the millisecond word is output, it will carry the tick. Acroamatics PCM decommutators generate the parity error bit and the not-in-lock bit. If your data is coming from some other source, the two status bits are whatever the external source puts in those two bits of the ID tag field.

The schematic of the data message is:

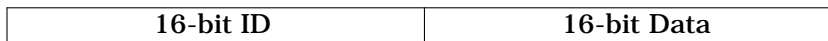


FORMAT 2:

Data and ID

The DIT consists of a 32 bit word. This format outputs the least significant 16 bits of the ID tag word exactly as received from the distribution system and 16 bits of data.

The schematic of the data message is:

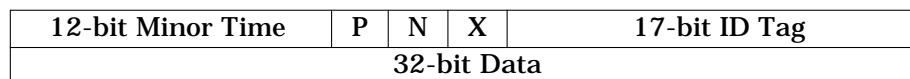


FORMAT 3:

Two Word Message with Minor Time

The DIT consists of two 32 bit words. The first word has three BCD digits of minor time microseconds of a millisecond in the twelve MSBs. The next two bits are the parity error and not-in-lock bits. The next bit is not used. The seven-teen LSBs are the ID tag. The second word is the long-word data. The PDSP positions short words in the sixteen LSBs and sign-extends them unless you specifically declare the output format to be USHORT or ULONG. If you declare it to be USHORT the PDSP sets negative values to zero. In any event, it then sets the sixteen MSBs to zero. Be sure to read the section *Output Conversions* later in this chapter if you use 32-bit output formats.

The schematic of the data message is:



FORMAT 4:

Data Only

The message consists of a 32 bit data word. When consecutive 16 bit words are output, the hardware packs the data into 32 bit words. When a 32 bit word is received and a 16 bit word is in the output packing register, the 16 LSB will be zero filled and output prior to formatting the 32 bit word.

SECTION 4 THEORY OF OPERATION

4.1 INTRODUCTION

The following paragraphs describe PDSP operation at the register level.

4.1.1 Setup & Initialization

A host computer initializes the PDSP card by executing instructions to VMEbus addresses that are memory mapped into 3MB of PDSP address space. The host uses the first MB to directly access the SHARC I/O registers and the internal RAM program and data memories. the second MB of address space accesses 17 32-bit words. The first 16 of these words set up the *Output Device Control Actel* chip, and the last address reads the *Test Data FIFO*. The third MB of address space accesses the 256k x 32 bit external RAM. The host uses this area to build a current value table.

The setup program initializes the external RAM and provides output device setup information prepared by the telemetry compiler. The host loads algorithm programs and a vector table into the SHARC memory. The host uses this vector table to access the programs from the algorithm selection OP-codes received from the 504VA Distribution card and processed by the *Distribution Actel* (which contains the circuits interfacing the 504VA Distribution card, and also performs the processing functions described below). The host then generates a software interrupt (by loading a specific I/O register) and the interrupt vector points to the start of the SHARC program. The program starts by trying to read *Distribution Actel Register 0*. If the distribution Actel has not received an OP-code, the *Transfer Acknowledge* signal is not set to **1** and the SHARC hangs in the input cycle. When processing an algorithm, the distribution first receives the 32-bit data word, followed by the ID tag, and fine time, and may also receive an OP-code word and, optionally, up to seven algorithm processing parameters. Information from the OP-code word is reformatted and sent to the SHARC as the first word of a message when the SHARC reads register 0. The SHARC continues to read register 0 until the entire OP-code message has been input. The message may contain from three to ten words.

4.1.2 Input OP-code Word

TABLE 4-1 shows the input OP-code word format.

OP-CODE WORD SCHEMATIC															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SPEC				DEST				OFORM				IFORM			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LO	COUNT			PROC		PORT		FL	OP-CODE						

TABLE 4-1. Input OP-code word.

The **OP-CODE** field contains a seven-bit code which identifies the operation the PDSP will perform. The *SPEC* field (bits 12-15) expands the OP-code field. The information is rearranged as shown in TABLE 4-3 to provide the OP-code in the

form required by the SHARC DSP. The OP-CODE addresses an entry table in the SHARC memory. The entry table contains a jump instruction to the code which executes the particular algorithmic function.

The **COUNT** field contains the length of the algorithm - which may be up to eight words including the OP-code word itself. The Distribution Actel uses this information to know when the message is complete

The **LO** field is the *Last Operation* field, which marks the last operation in a list of operations you want to perform on a given data sample. This bit is not used by the SHARC PDSP.

The **PROC** field selects which processor will perform an algorithm. This bit is also not used by the SHARC PDSP.

The **PORT** field selects which output port will receive the data. The *Output Processing* Actel uses these bits, along with the *Output Destination* and *Output Format* fields,

The **FL** field is a one-bit flag which controls the operation of an algorithm. In the standard algorithm the FL field is a *Chained Algorithm* bit, and tells the SHARC to use the data from the previous algorithm, rather than re-reading the current input data, to obtain data to process.

You can specify the **PROC**, **PORT**, and **FL** fields in the template so that the process will be permanently assigned to a selected processor, or the output port permanently selected, or the flag set to a specific value. If permitted by *modifier enables*, these fields may also be filled in when the algorithm is invoked, using the commands

USE P_n to select the processor
or
OUT CH_n to select the port bits

You can set the Flag bit for the current algorithm invocation by preceding the algorithm name with an ampersand.

You use the **SPEC** field to expand the OP-CODE field of the OP-code word to increase the number of possible algorithms.

DEST specifies which of 16 possible output destinations you wish to send the data to (eleven of these are presently defined). The Compiler can set this field according to the value of a global specifier which you include in your program file. The two port bits are also sent to the output device. Some output devices use these bits to direct the data to multiple output channels.

OFORM specifies the desired output format of the data. Of the sixteen possible formats, eleven are at present defined. The Compiler can set this field according to the value of a global specifier which you include in your program file, or by a specifier included in the algorithm invocation.

IFORM specifies the input format of the data. Again, of the sixteen possible formats, nine are presently defined. The Compiler can set this field according to the value of a global specifier which you include in your program file.

Except for the **SPEC** field, the Compiler can modify the OP-code word when the algorithm invocation is compiled. This allows you to specify the input and output formats, as well as the output destination. A zero in a nibble of an OP-

code word, as defined in the template, permits that field to be overwritten by a globally defined specifier. If the field is non-zero, that nibble is “canned” into the template and cannot be changed.

The three fields which you can specify have the coding shown in the following table. Each column is independent - although shown in the same table, there is no relation across rows between fields, other than the value number.

OP-CODE WORD CODING						
Value	DEST		OFORM		IFORM	
0	DV1	Device 1	SHORT	Signed 16 bit	2CM	Two's Comp
1	DV2	Device 2	OBN	Offset Binary	OBN	Offset Binary
2	DV3	Device 3	1CM	One's Comp	1CM	One's Comp
3	DV4	Device 4	SMG	Signed Mag	SMG	Signed Mag
4		Feedback Port	USHORT	Unsigned 16 bit*	UNS	Unsigned 16 bit*
5	DV5	Device 5	ULONG	Unsigned 32 bit*	BCD	Binary coded decimal*
6	DV6	Host Input	LONG	Signed 32 bit	LONG	Signed 32 bit
7		DAC Bus	IEF	IEEE float	IEF	IEEE float
8	DV8	Serial Out				
9	DV9	DMA				
A	Reserved		MIL	MIL-STD float*	MIL	MIL-STD float*
B	Reserved		HIGH	16 msb's of a long	NONE	
C	Reserved		LOW	16 lsb's of a long	NONE	
D	Reserved			NONE	NONE	
E	Reserved			NONE	NONE	
F	No Output			NONE	NONE	

* These data types set the special conversion flag.

TABLE 4-2. OP-code Destination, Input, & Output Data Format Coding.

4.1.3 Output OP-code Word

TABLE 4-3 shows the output OP-code word format as it is sent to the SHARC.

OP-CODE WORD SCHEMATIC																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
NOT		OF	IF	DEST				OFORM				IFORM				
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
PORT		OP-CODE										SPEC				0

TABLE 4-3. Output OP-code Word.

The SHARC uses the first 12 bits of the OP-code to form an address to a *vector table* that contains jump instructions to the address of the appropriate algorithm processing routine. When the OP-code is received, the distribution Actel examines the input and output format fields to determine if the Actel chips can perform the required data type conversions, or if it requires the SHARC to do them. If the conversions require the SHARC DSP, bit zero is set to **1** to modify

the vector address, thus performing the required data conversions as a part of the processing algorithm. We also use the input data format field to control the IF flag in OP-code word bit 28. Bit 28 is set to **1** if the input data is in IEEE floating point notation. The OF flag in bit 29 is controlled by the output data format and is set to **1** when the output data is to be in IEEE floating point format. When the input conversions are simple, the distribution Actel performs the data conversion. The Port bits, IFORM, OFORM and Destination fields are sent to the SHARC. As the SHARC reads the OP-code, the output device Actel *snoops* the OP-code word and uses the output form, device, and port bit to format and direct any resulting data messages.

4.1.4 SHARC Algorithm Message

The SHARC continues to read the distribution Actel register 0 to input the information required by the algorithm. The message following the OP-code contains the ID and Fine Time word, the data word, and up to seven words as required by the algorithm.

4.1.5 ID Word

The 504VA Distribution card broadcasts the ID tag (with status and fine time included) and the 32 bit data sample prior to outputting and OP-code word. When the SHARC has read the OP-code word, the distribution Actel prepares to output the ID word on the SHARC next read of register 0. When the SHARC reads this word the output device Actel snoops the word and saves the ID tag, status and fine time to use if required by the device output format when SHARC output messages are processed.

4.1.6 Data Words

The data word transferred to the SHARC may be the input data, the input data with data type conversions accomplished, or for chained algorithms the data output by the preceding algorithm. The SHARC must output a data word to indicate that the current algorithm is completed. When the algorithm results in an output message the SHARC writes the data to the output device Actel register zero. The distribution Actel snoops this message and saves the data for use when the following OP-code has the chained flag set. When the algorithm does not result in an output message, the SHARC outputs the processed data to the distribution Actel by writing register zero. This indicates that the current algorithm is complete and provides the processed data that will be returned to the SHARC as input data when chained algorithms are output.

4.1.7 Input Data Conversion

The binary data that is processed by the PDSP is usually produced by an analog to digital converter. The converter generates a specific binary output for a given analog input, however these converters vary widely in design, produce a variety of binary word sizes, and numerous binary output codes. Frequently, unipolar converters are used to measure bipolar signals and bipolar converters are used to measure unipolar signals. This is accomplished by offsetting the analog signal so that it lies in the optimum conversion range. When you process such data with the TDP, you generally want to convert it to properly ranged *two's complement* data. Two's complement representation is used for computations by the PDSP, as well as by any host computer that processes the TDP data output.

The distribution Actel has the following conversions for sixteen bit fixed point data. (This is the data format that we call a *SHORT*.) The resulting words are passed to the SHARC as 32 bit words.

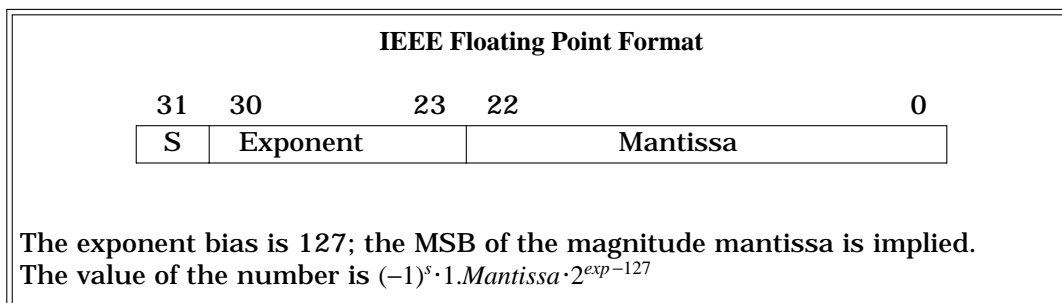
- a. **Two's Complement (IFORM0)**
Incoming two's complement data is passed to the PDSP unchanged. We use bit 15 to sign extend the word to 32 bits.
- b. **Offset Binary (IFORM1)**
Measuring bipolar signals with unipolar devices generates offset binary data. The conversion to two's complement is done by inverting the sign bit, effectively removing the half of full scale offset that was applied to the data when it was measured. This results in a one's complement word that is converted to two's complement by incrementing negative values by one count. We use bit 15 to sign extend the word to 32 bits.
- c. **One's Complement (IFORM2)**
Incoming one's complement data is converted to two's complement by incrementing negative values by one count. We use bit 15 to sign extend the word to 32 bits.
- d. **Sign and Magnitude (IFORM3)**
This type of data is converted by two's-complementing all bits except the sign bit, if the sign bit is a one. We use bit 15 to sign extend the word to 32 bits.
- e. **Unsigned 16 Bit (IFORM4)**
When the measured data is unipolar and the data uses the full converter range, the result will be a positive 16 bit integer. When the data is declared as unsigned, the data is passed unchanged (bit 15 is not sign extended into the 16 most significant bits of the data). Use this input format to leave non-analog data unmodified.
- f. **BCD Data (IFORM5)**
Occasionally you may need to process data from a BCD converter. You can specify BCD input conversion, but the result is an integer in the range 0-9999. This word is passed unmodified to the SHARC, which performs the BCD to binary conversion.

The *LONG* words in the input stream are normally produced by a computer and are either 32 bit two's complement or a floating point representation of the data. All long words are passed to the SHARC unaltered. The special input or output conversion required flag in bit 0 of the SHARC OP-code word is set to **1** when the *input* format is IFORM4, 5, 8, 9 or A, and when the *output* format is OFORM4, 5, 8, 9, or A. Two additional format flags are generated for the SHARC OP-code word bit 28 and 29. Bit 28 is set to **1** when the input word is an IEEE floating point value (IFORM7, 8, 9, or A. Bit 29 is set to **1** when the output word is a floating point value (OFORM7, 8, 9, or A). The long input formats are as follows.

- g. **Long 32 Bit Word (IFORM6)**
The input word is passed to the SHARC unchanged.

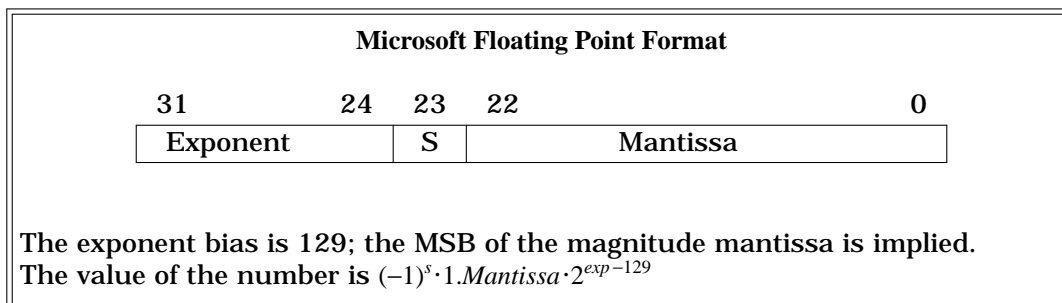
h. IEEE Standard 754 Floating Point Format (IFORM7)

The IEEE format is the internal operating format of the SHARC, so this is the system in which all floating point computations are performed in the PDSP. The number is calculated as shown below.



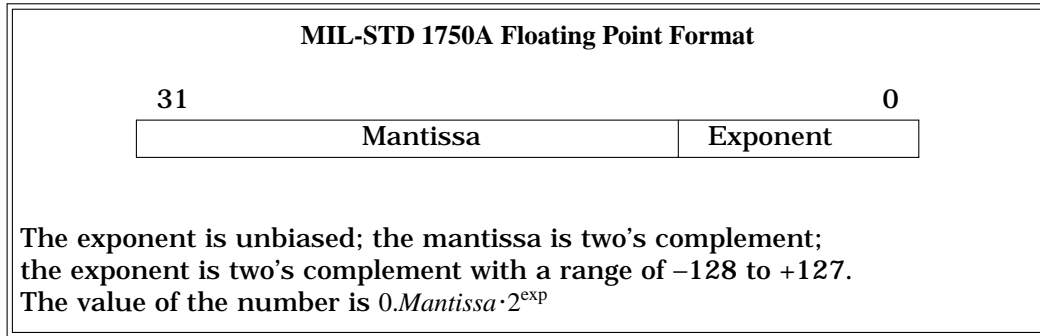
i. MICROSOFT Floating Point Format (IFORM8)

The Microsoft format was invented by Microsoft for their BASIC Interpreters. The format was imported to their earlier C Compilers for MS-DOS Systems, although they have now abandoned it in favor of the IEEE format. The SHARC will convert data from this format on input and to this format on output. If you chain algorithms FROM an algorithm that outputs in Microsoft format, you must state the input format for the chained algorithm as IFORM8.



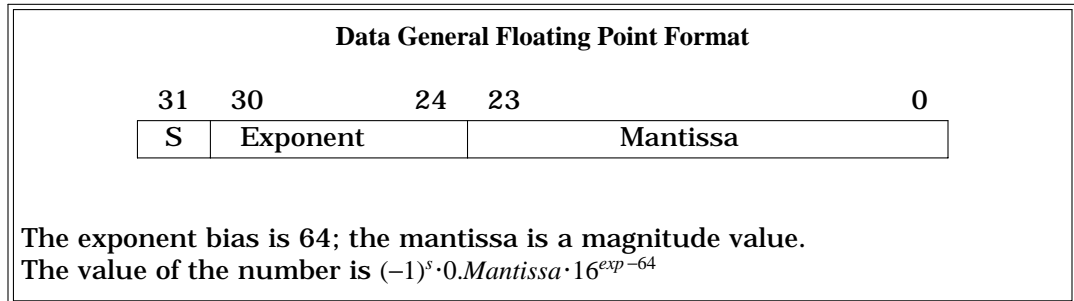
j. MIL-STD 1750A Floating Point Format (IFORM9)

The Mil Standard format is that used by systems that must conform to the computational standards imposed by the Department of Defense, particularly those systems using ADA. The SHARC will convert data from this format on input and to this format on output. If you chain algorithms FROM an algorithm that outputs in MIL-STD format, you must state the input format for the chained algorithm as IFORM9.



k. DATA GENERAL Floating Point Format (IFORMA)

The Data General format is used by Data General programming systems as well as by other mainframe systems. It has the advantage of a very large range of values (for which it sacrifices precision of the mantissa). The exponent is the power of 16 rather than the power of two used by the other formats. This means that the mantissa must be normalized relative to sixteen and that its MSB need not be 1, even when it is normalized. If you chain algorithms from an algorithm that outputs in Data General Floating Point Format, you must state the input format for the chained algorithm as IFORMA.



4.1.8 CONDITIONAL ALGORITHM SEQUENCE

The SHARC executes a *Conditional Algorithm*, a series of algorithms in which the execution of the present algorithm is determined by the results of the conditions found in the preceding algorithm. This series of algorithms is terminated with a reserved OP-code that ends the series regardless of conditions encountered in preceding operations. The Distribution Actel provides hardware to enhance the throughput of these algorithms as follows. When the SHARC executes a conditional algorithm and the conditions indicate that the remaining algorithm in the series need not be executed, the SHARC outputs a data word to the Output Device Actel or, if no data output is required, the current data value is written in register zero on the distribution Actel (this is the normal sequence that indicates the end of each algorithm). During this data store operation the SHARC sets Flag Line One to a 1, which indicates to the Distribution Actel that this is not only the end of an algorithm but also the completion of a conditional sequence. The Distribution Actel responds by discarding any following OP-codes and their parameters until an OP-code word with the reserved value is found. This special OP-code word is transferred to the SHARC, which completes the conditional

algorithm and resumes normal operation.

4.2 SHARC DSP

The SHARC function is to receive data, ID tags, and algorithms from the Distribution Actel by reading register zero, and to then process the data as required by the algorithm. BCD data is converted to binary and non-standard floating point to IEE754 format. When the input data is in integer format, it is converted to floating point and when the input is floating point it is converted to integer, thus creating the type of data required by the algorithm. When the algorithm produces a conditional output such as data compression or Output Sample *n*, the SHARC tests Input Flag Zero, which is the Force Data Flag generated by the 504VA Distribution card and passed through the Distribution Actel. When flag zero is set to **1** the data is output regardless of other criteria. When the algorithm does not require data to be output, the current integer value of the data is written to the distribution Actel register zero to indicate that the algorithm has been processed. This write operation also allows the distribution Actel to start the next algorithm outputting process if a new OP-code has been received. The distribution Actel checks the chained algorithm bit in the input OP-code and if set returns the data output from the SHARC as the next input data when the SHARC reads the next algorithm set. The algorithm always starts with an OP-code followed by an ID and data word. Many algorithms also contain a re-tag IDS word and the required processing parameters.

4.2.1 SHARC Output Format

Data that is output by the SHARC is conditioned by the algorithm being executed, the input data format, and the output data format. The SHARC uses flags in the OP-code to determine if an input or output data conversion is required, if the input data is floating format or integer, and whether the output data will be an integer or floating format. The output message is sent to the output device Actel by writing one of eight addressable registers. Flags two and three also provide output formatting. The address and flag usage is shown in TABLE 4-3 below.

OUTPUT DEVICE FLAGS & REGISTER ADDRESSES		
Address	Description	
0	Write Address for:	Normal Data Output
1	"	ID Tag Output
2	"	Binary Time milliseconds of Day
3	"	Binary Time Days of Year
4	"	16 Bit Word
5	"	16 Bit Word with last flag
6	"	32 Bit Word
7	"	32 Bit Word with last flag
8	"	4 Bit Word to select output device
9	"	Unused Word, writing it sets tick flag
Flag 2	Start Of Frame flag	
Flag 3	End Of Process flag	

TABLE 4-4. Output Device Control Flags & Register Descriptions.

4.2.2 Normal Message Outputs

When the SHARC outputs a normal data word, the value is written into output device Actel register zero. The output device Actel will format the message for the device specified in the OP-code word and transfer the data to the specified device. When the output message format requires an ID tag, the tag may be specified by the SHARC by writing the tag to address 01 prior to sending the data. The ID tag may be 12 to 17 bits long as required by the output format. When the output format requires status or fine time as part of the message, the information snooped from the input ID word will be used. When address 01 is not written prior to the data output, the values from the input ID word will be used for the message formation. The output message to the device may be required to start transferring data synchronously to an input source. When this is required, that device control register is enabled in synchronous mode and will not start the output message until an output word for that device is received with the Start of Frame flag (Flag 2) set to 1.

4.2.3 Binary Time Message

The *Output Device Actel* generates an output format that may require binary time as a time stamp in blocked output format. When you require binary time, you program the SHARC to convert the *BCD milliseconds word* (containing milliseconds, seconds, minutes, hours and days) to produce *binary milliseconds of day* and *binary day of year* messages. The milliseconds word is loaded into output device Actel *Register 2* and the days word in *Register 3*. The output Actel holds the binary time in internal registers for use when the output format requires a binary time stamp.

4.2.4 Custom Algorithm Output Data

Custom algorithms may generate output data that is not formatted by the output device Actel. The SHARC must know the size of the bus that the output device uses and if the device is on the A-bus. The last word flag must be sent with the last word of an A-bus message. Sixteen bit words are output to output Device Actel register four, and 32-bit words are output to register six. When the word is the last word of a packet sent to the A-bus, the last word flag must be set to 1. This is indicated by sending the last 16 bit word of a message to register five or for a 32-bit word to register seven.

4.2.5 End Of Process (Flag 3)

When the output device Actel is programmed to output a blocked format it counts down a fixed number of words then sends the last word of the block with the EOP signal. This signal is used by several external devices to terminate the current block transfer and begin a new block. When the SHARC executes output algorithms **PLW**, **PLWT**, & **QEOF**, it generates Flag 3, which will cause the output device Actel to transmit the word to the output device with the EOP line set to 1. These algorithms also cause the output formatting hardware to reset these block length counter and if enabled, output a block header message with the next word transmitted.

SECTION 5

PDSP - SWITCH & JUMPER SETTINGS

5.1 DESCRIPTION

The paragraphs below describe the selections available on the 505VA PDSP (6011505-10) card.

5.1.1 A16 Address Select

Two 16-bit registers are located on the PDSP Card and are mapped in the A16:D16 memory address space of the VME Host computer. Switches U31 and U27 select the base address of a 40 byte register block. Switch positions 8 through 1 of U31 determine the eight MSBs of the address, A15 through A8; switch positions 1 & 2 of U27 set the LSBs address bits A7 and A6. Switches 3-8 of U27 perform other functions described below.

5.1.2 Factory Settings

Pages 5-4 & 5-5 show the default factory settings of jumpers and switches on the PCB. Pages 5-6 & 5-7 show the switch functions.

5.1.3 U27 - DMA Address Mode

Switch 3 of U27 selects the address mode for DMA transfers. Switch 3 ON selects A32 mode: OFF selects A24 mode.

5.1.4 U27 - Interrupt Acknowledge Level

U27 switches 6-8 select the Interrupt Acknowledge level. The switches are coded in binary with switch 6 the MSB and switch 8 the LSB. These switches must be set to the same interrupt level as the Interrupt Request level (JP4) selection.

5.1.5 U27 - On Board Memory Size

U27 switches 4-5 are set to match the size of the CVT memory installed on your card. Switch 4 must be set to ON and switch 5 set to OFF (5505) to indicate the extended memory option of 4MB of SRAM. Switch 5 set ON 94505) indicates the standard memory option of 1 MB SRAM.

5.1.6 JP1, JP3 - DMA Bus Grant & Request

JP1 selects the bus grant level for DMA transfers. The Bus Grant In, Bus Grant Out, and Bus Request (selected by JP3) must all be set to the same level. JP1 also selects Bus Grant Passthrough, and you must place the bus levels not used by the DMA in the Bypass position.

5.1.7 JP2 - A-bus Request and Acknowledge

JP2 selects the request and acknowledge priority level on the A-bus. The bus request and acknowledge signals must have matching priority levels.

5.1.8 JP4 - Interrupt Request Level

JP4 selects the Interrupt Request level. Install the jumper corresponding to the interrupt level you want. Note that the Interrupt Acknowledge level (set with switch U27 above) and the Interrupt Request level must match.

5.1.9 JP5 - HOTLink™ Self Test Mode

JP5 selects between the Self Test and Normal Operation modes of the HOTLink™. Installing the jumper selects the self test mode.

5.1.10 JP7, JP8 - D-bus Priority Selection

JP7 jumpers 9-10, 11-12, 13-14, and 15-16 correspond to the D-bus OPcode clock levels. JP8 jumpers 9-10, 11-12, 13-14, and 15-16 correspond to the D-bus Ready for OPcode levels. The jumpers must select matching levels. Jumpers 1-8 on JP7 and JP8 are unused.

5.1.11 JP9, JP10 - HOTLink™ Output Data Type

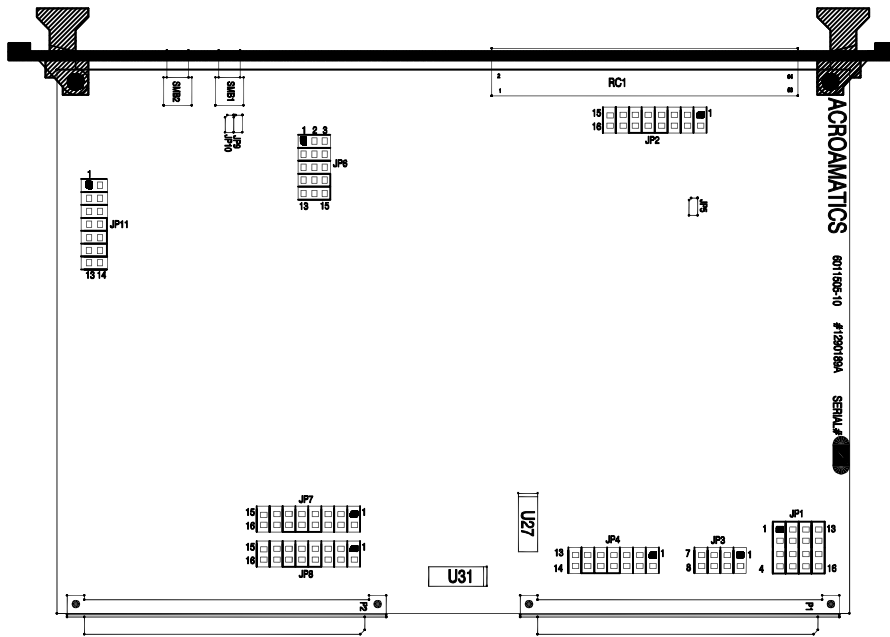
JP9 and JP10 select the output of of HOTLink™ data as either single ended or differential.

5.1.12 JP6 - On Board Clock Setting

This jumper is set at the factory.

5.1.13 JP11 - SHARC (DSP) JTAG connection

This connection is the DSP chip JTAG interface, and sets the Normal mode when installed.



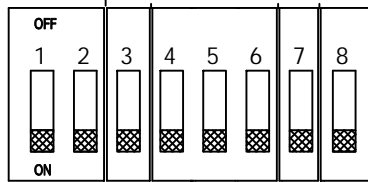
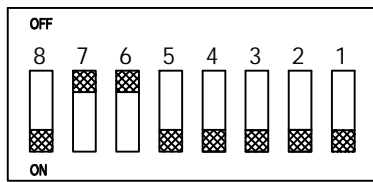
ADDRESS 600X SHOWN

A15 ←

A6

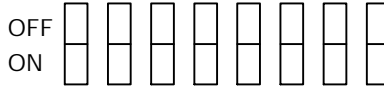
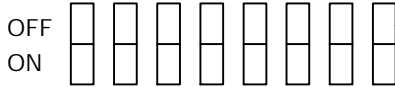
SEE PAGE 5-1 & 5-5

OFF = 1
ON = 0



U31

U27



SHIPPED ADDRESS _____

CARD 6011505-11 _____

SERIAL# / REV. _____

CUSTOMER _____ JOB# _____

CONFIGURED BY _____ DATE _____

QC CHECK BY _____ DATE _____

JP1

PINS	INSTALLED
1-5	
2-6	
3-7	
4-8	
9-13	
10-14	
11-15	
12-16	
5-9	
6-10	
7-11	
8-12	

JP2

PINS	INSTALLED
1-2	
3-4	
5-6	
7-8	
9-10	
11-12	
13-14	
15-16	

JP3

PINS	INSTALLED
1-2	
3-4	
5-6	
7-8	

FIGURE 5-1A. VME DATA STREAM PROCESSOR 1MB #6011505-11-PDSP FACTORY SETTINGS.

JP4

PINS	INSTALLED
1-2	
3-4	
5-6	
7-8	
9-10	
11-12	
13-14	

JP5

PINS	INSTALLED
1-2	

JP6

PINS	INSTALLED
11-12	FACTORY INSTALLED

JP7

PINS	INSTALLED
1-2	
3-4	
5-6	
7-8	
9-10	
11-12	
13-14	
15-16	

JP8

PINS	INSTALLED
1-2	
3-4	
5-6	
7-8	
9-10	
11-12	
13-14	
15-16	

JP9

PINS	INSTALLED
1-2	

JP10

PINS	INSTALLED
1-2	

JP11

PINS	INSTALLED
1-2	
3-4	
5-6	
7-8	
9-10	
11-12	
13-14	

CARD #6011505-11 _____

FIGURE 5-1B. VME DATA STREAM PROCESSOR 1MB #6011505-11 (PDSP) FACTORY SETTINGS.

JP1 - VME BUS GRANTS

PINS	FUNCTION
1-5	BUS GRANT IN 0 SELECT
2-6	BUS GRANT IN 1 SELECT
3-7	BUS GRANT IN 2 SELECT
4-8	BUS GRANT IN 3 SELECT
9-13	BUS GRANT OUT 0 SELECT
10-14	BUS GRANT OUT 1 SELECT
11-15	BUS GRANT OUT 2 SELECT
12-16	BUS GRANT OUT 3 SELECT
5-9	BYPASS BG IN 0 TO BG OUT 0
6-10	BYPASS BG IN 1 TO BG OUT 1
7-11	BYPASS BG IN 2 TO BG OUT 2
8-12	BYPASS BG IN 3 TO BG OUT 3
THE THREE UNSELECTED BUS GRANTS MUST BE BYPASSED	

JP2 A-BUS REQUEST AND ACKNOWLEDGE

PINS	FUNCTION
1-2	A-BUS OUTPUT ACKNOWLEDGE 3
3-4	A-BUS OUTPUT ACKNOWLEDGE 2
5-6	A-BUS OUTPUT ACKNOWLEDGE 1
7-8	A-BUS OUTPUT ACKNOWLEDGE 0
9-10	A-BUS OUTPUT REQUEST 3
11-12	A-BUS OUTPUT REQUEST 2
13-14	A-BUS OUTPUT REQUEST 1
15-16	A-BUS OUTPUT REQUEST 0

JP3 - VME BUS REQUEST

PINS	FUNCTION
1-2	BUS REQUEST 0 SELECT
3-4	BUS REQUEST 1 SELECT
5-6	BUS REQUEST 2 SELECT
7-8	BUS REQUEST 3 SELECT

NOTE: BUS REQUESTED, BUS GRANT IN,
& BUS GRANT OUT MUST MATCH

JP4 - VME INTERRUPT REQUEST

PINS	FUNCTION
1-2	INTERRUPT REQUEST 1 SELECT
3-4	INTERRUPT REQUEST 2 SELECT
5-6	INTERRUPT REQUEST 3 SELECT
7-8	INTERRUPT REQUEST 4 SELECT
9-10	INTERRUPT REQUEST 5 SELECT
11-12	INTERRUPT REQUEST 6 SELECT
13-14	INTERRUPT REQUEST 7 SELECT

NOTE: INTERRUPT REQUEST LEVEL ON
JP4 MUST MATCH INTERRUPT LEVEL
SELECTED ON U27

FIGURE 5-2A. 505VA (PDSP) SELECTIONS

JP7 D-BUS OPCODE CLOCK PRIORITY SELECTION

PINS	FUNCTION
9-10	OPCODE CLOCK PRIORITY 4
11-12	OPCODE CLOCK PRIORITY 3
13-14	OPCODE CLOCK PRIORITY 2
15-16	OPCODE CLOCK PRIORITY 1

JP8 D-BUS READY FOR OPCODE SELECTION

PINS	FUNCTION
9-10	READY FOR OPCODE 1
11-12	READY FOR OPCODE 2
13-14	READY FOR OPCODE 3
15-16	READY FOR OPCODE 4

SWITCH U27			DISPLAY
6	7	8	Description
on	on	on	Interrupt acknowledge level 7
on	on	off	Interrupt acknowledge level 6
on	off	on	Interrupt acknowledge level 5
on	off	off	Interrupt acknowledge level 4
off	on	on	Interrupt acknowledge level 3
off	on	off	Interrupt acknowledge level 2
off	off	on	Interrupt acknowledge level 1
off	off	off	Interrupt acknowledge level

FIGURE 5-2B. 505VA (PDSP) SELECTIONS

SECTION 6 DRAWINGS

6.1 INTRODUCTION TO THE DRAWINGS

Section 6 contains a complete technical drawing package describing your VME card. The drawings in this section are keyed to your specific serial numbered card.

6.1.1 Drawing System

Acroamatics Drawing numbers are seven digit numbers which can also have a two digit dash number. The first four digits represent a drawing class, and wherever a drawing may be part of a standard drawing package, drawing numbers are issued so that all drawings which are part of the package share the same last three digits. In the following discussion "xxx" represents the number keyed to the the card part number (6011xxx). Individual parts are classified within the same drawing system, but are assigned serially without regard to other assemblies.

The PC Card Reference package includes the following drawings:

FOR CARD PART NUMBER 60115xx:

60115xx	Card Assembly Drawing
81115xx	Card List of Materials
21115xx	Card Schematic Drawing

6.1.2 Drawing Package Organization

This section of the manual contains the physical drawings, called *Drawings*, as opposed to the schematic drawings, called *Schematics*, which are found in Section 7.

The Drawings section includes the card component assembly drawing 60115nn and the card List Of Materials (LOM). LOM's include sufficient information to facilitate ordering replacement parts either from Acroamatics or from the original component manufacturer. LOMs list parts by Acroamatics Part Number in the column headed *PART NO*. The component manufacturer is identified as *VENDOR*. Parts for which ACROAMATICS is listed as vendor are proprietary components available only from Acroamatics, Inc. Integrated Circuits which are industry standard are listed as *GENERIC*, and may be obtained from any reliable vendor. Other parts for which a specific source is listed may be available from other sources. When substituting parts from vendors other than those specifically listed, be certain that the components are truly interchangeable.

The last column (Reference) of the List of Materials lists the assembly location or locations. An assembly location can contain a socket as well as the component plugged into the socket.

For example

U15
S1
74ALS244

This example shows that location U15 contains socket S1 and an IC of type 74ALS244. Resistors, capacitors, and other components are shown in a similar fashion, and are referenced using common industry abbreviations.

6.1.3 Programmed Parts

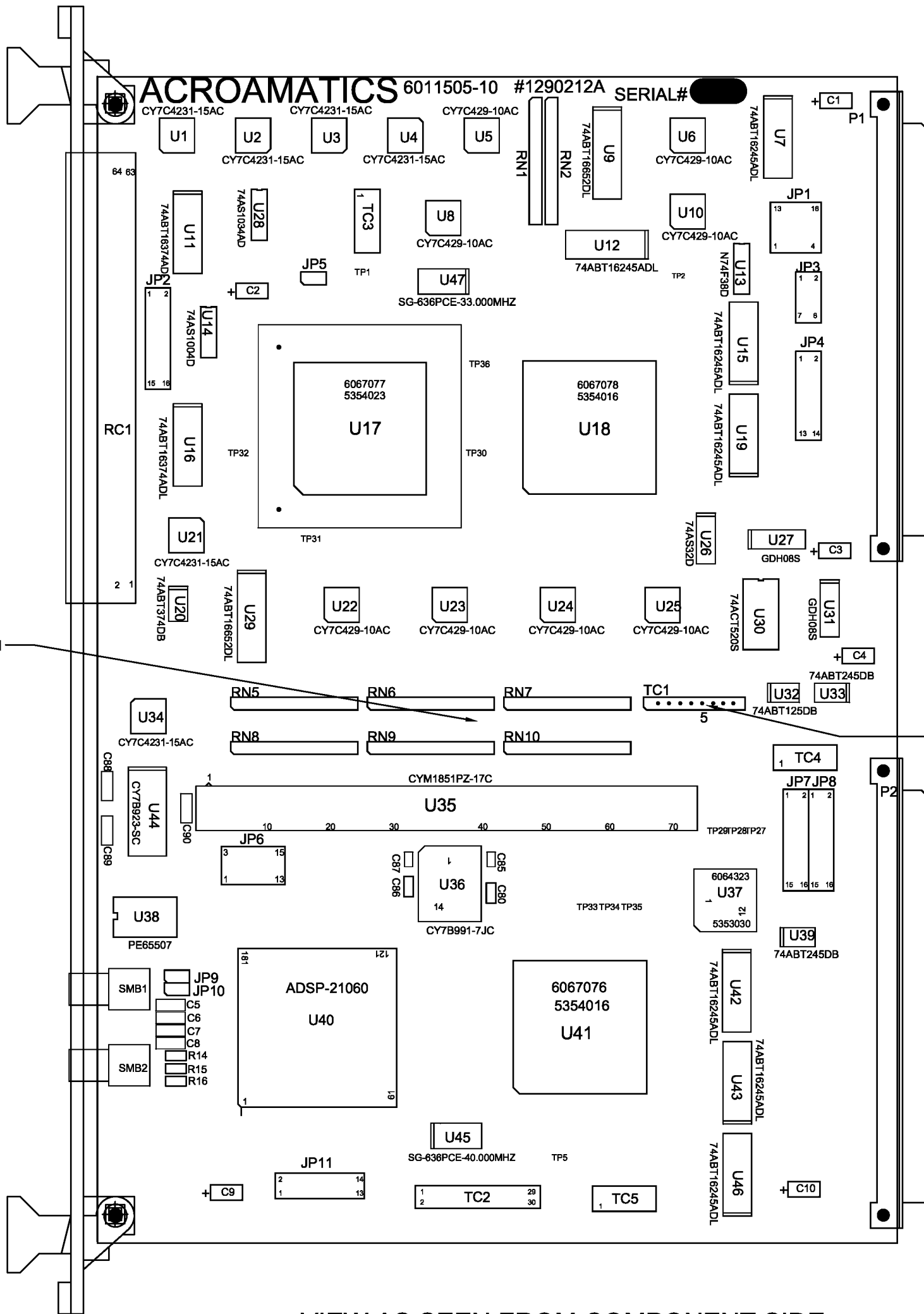
The VME card can include programmed parts such as PROMs, EPROMs, EEPROMs, PALs, GALs, FPGAs, etc. If these are a permanent part of the hardware, they are documented on the List Of Materials for the PC card on which they are installed. Programmed parts are listed on the LOM twice; once as the unprogrammed part, with the Manufacturers Part Number, and also under the Acroamatics program number (606xxxx) with which they must be programmed to become the correct programmed part.

Programs for PROMs have part numbers in the series 6061xxx

Programs for EPROMs and EEPROMs have part numbers in the series 6062xxx

Programs for PALs and GALs have part numbers in the series 6064xxx

Programs for FPGAs have part numbers in the series 6067xxx

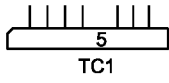


NOTE 1

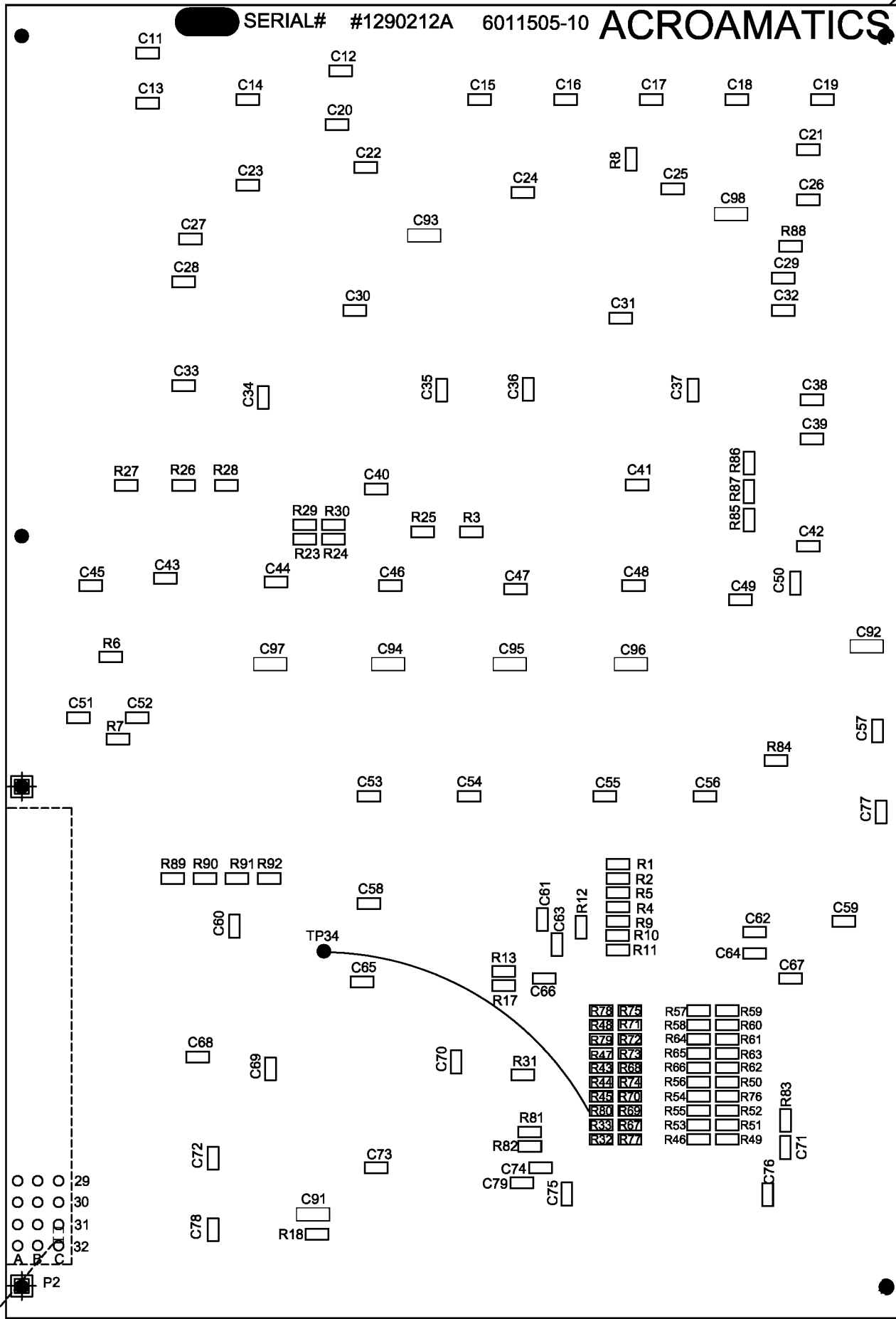
NOTE 3

VIEW AS SEEN FROM COMPONENT SIDE

- NOTES:
1. ALIGN PIN 1 OF SIP RESISTORS (RN6, RN7, RN9, RN10) WITH PAD 1 AT LOCATIONS (RN6, RN7, RN9, RN10). LEAVE PAD 10 UNUSED.
 2. INSTALL TEST POINTS (TP1, TP2, TP5, TP27, TP28, TP29) ONLY. LEAVE ALL OTHER TEST POINT LOCATION EMPTY.
 3. CUT PIN 5 OF TC1 AS SHOWN IN DRAWING.



DR	B. GALAZIOS	2/04	ACROAMATICS <small>TELEMETRY SYSTEMS</small> GOLETA, CAL. 93117		
CHK					
A P P D			ASSEMBLY, CIRCUIT CARD PROGRAMMABLE DATA STREAM PROCESSOR		
NEXT ASSY	USED ON		SIZE	SCALE	DWG NO.
			B	NTS	6011505-10
APPLICATION			SHEET	2 OF 3	REV L



VIEW AS SEEN THROUGH COMPONENT SIDE

SOLDER D1 ON TOP OF PINS C32 & C31 OF P2 CONNECTOR
MAKE SURE THE CATHODE IS ON C32 PIN

NOTE: SOLDER WIRE FROM TP34 TO R80 AS SHOWN

DR B. GALAZIOS 2/04		ACROAMATICS <small>TELEMETRY SYSTEMS GOLETA, CAL. 93117</small>	
CHK		ASSEMBLY, CIRCUIT CARD	
A P P D		PROGRAMMABLE DATA STREAM PROCESSOR	
NEXT ASSY		SIZE B	DWG NO. 6011505-10
USED ON		SCALE NTS	REV L
APPLICATION		SHEET 3 OF 3	

**LIST OF MATERIALS
VME PDSP (4MB)**

8111505-10

PAGE 1 OF 2

ASSEMBLY PN 6011505-10

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ENGINEERING APPROVAL _____ DATE _____

MANUFACTURING APPROVAL _____ DATE _____

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
1	1290212	1	PCB VME PDSP	1290212	ACROAMATICS	
2	2796061	2	CONN PC 96P SDR RTANGL	7296-50C2TH	3M	P1,P2
3	2796060	1	CONN PC 64P SDR RTANGL	2564-5002UB	3M	RC1
4	2796057	2	CONN PC SMB RTANGLE 1P	903-373J-51A	AMPHENOL	SMB1,SMB2
5	2796101	1	CONN PC 30 PIN HEADER SMT	DF13-30DP-1.25	HIROSE	TC2
6	2796104	3	CONN PC 7PIN 1.25 HEADER SMT	53398-0790	MOLEX	TC3,TC4,TC5
7						
8						
9	3573821	1	DIODE SCHOTTKY SMT 200mA	MA2SD10CT-ND	PANASONIC	D1
10						
11	1903063	11	CAP TMP STBL (X7R) .022uF SMT	ECU-V1H223KBM	PANASONIC	C88-C98
12	1903069	71	CAP X7R .1uF 5% 50V SMT-805	C0805C104J5RAC	KEMET	C11-C80,C86
13	1922643	6	CAP TA 10uF 10% 16V SMT	T491B106016AS	KEMET	C1-C4,C9,C10
13			Acceptable substitute is:	ECS-T1CX106R	PANASONIC	
14	1904101	4	CAP NPO 1000pF 50V SMT 1206	ECU-V1H102JCH	PANASONIC	C5-C8
15	1904106	2	CAP NPO 100pF 5% 50V SMT	ECU-V1H101JCV	PANASONIC	C85,C87
16						
17	7680974	5	RES 121 OHM .1W 1% SMT-0805	ERJ-6ENF121	PANASONIC	R2,R5,R10,R12,R13
18	7680975	5	RES 39.2 OHM .1W 1% SMT-0805	ERJ-6ENF39.2	PANASONIC	R1,R4,R9,R11,R17
19	7680979	27	RES 1K .1W 1% SMT-0805	ERJ-6ENF1.00K	PANASONIC	R6,R31,R45-R69
20	7680980	3	RES 33.2 OHM .1W 1% SMT-0805	ERJ-6ENF33.2	PANASONIC	R85,R86,R87
21	7680981	35	RES 10K .1W 1% SMT-0805	ERJ-6ENF10.0K	PANASONIC	R7,R8,R18,R23-R30,R32,R33 R43,R44,R70-R84,R88-R92
21						
22	7680988	4	RES 267 OHM .1W 1% SMT-0805	ERJ-6ENF267	PANASONIC	R3,R14,R15,R16
23						
24	7700036	4	RES SIP 1.5K/3.3K 10P 2%	CSC10A05-152/332-G	DALE	RN1,RN2,RN5,RN8
25	7700055	4	RES SIP 1K 8R 9P LOW PROFILE	CSC09A-01-102G	DALE	RN6,RN7,RN9,RN10
26	5300004-42	1	IC HEX INVERTER (SMD)	74AS1004D	GENERIC	U14
27	5300034-37	1	IC HEX DRIVER +-48ma SMT	74AS1034AD	GENERIC	U28
28	5300038-39	1	IC QUAD 2-INP NAND BUFF(SMD)	N74F38D	GENERIC	U13
29	5300032-91	1	IC QUAD 2-INP OR GATE SMT	74AS32D	GENERIC	U26
30	5300125-49	1	IC QUAD BUF NI INDEP-TS SMT	74ABT125DB	GENERIC	U32
31	5300245-55	7	IC 16BIT BUS XCVR SMT NI TS	74ABT16245ADL	GENERIC	U7,U12,U15,U19,U42,U43,U46
32	5300245-91	2	IC OCT BUS XCVR NI TS SMT	74ABT245DB	GENERIC	U33,U39
33	5300374-55	2	IC 16BIT D-F/F EDGE-TRIG SMT	74ABT16374ADL	GENERIC	U16,U11
34	5300374-91	1	IC OCT D-F/F EDGE-TRIG SMT	74ABT374DB	TI	U20
34			Acceptable substitute is:	74ABT374CMSA	NATIONAL	
35	5300520-63	1	IC 8-BIT MAG COMP SMT	74ACT520S	NATIONAL	U30
36	5300652-55	2	IC 16BIT BUS XCVR W/RGSTRS TS	74ABT16652DL	GENERIC	U9,U29
37	5308003	1	IC 160-330MBPS SERIAL XMIT	CY7B923-SC	CYPRESS	U44
38	5308991	1	IC PROGRAMMABLE SKEW CLK BUF	CY7B991-7JC	CYPRESS	U36
39	5308429-10	8	IC 2Kx9-BIT FIFO (QFP)	CY7C429-10AC	CYPRESS	U5,U6,U8,U10,U22-U25
40	5308423-15	6	IC 2Kx9 SYNCHRONOUS FIFO SMT	CY7C4231-15AC	CYPRESS	U1,U2,U3,U4,U21,U34
40			Acceptable substitute is:	IDT72231L15PF	IDT	
41	6128060	1	IC 32-BIT DSP COMPUTER 40M	ADSP-21060KS-160	ANALOG-DEVICE	U40

**LIST OF MATERIALS
VME PDSP (4MB)**

8111505-10

PAGE 2 OF 2

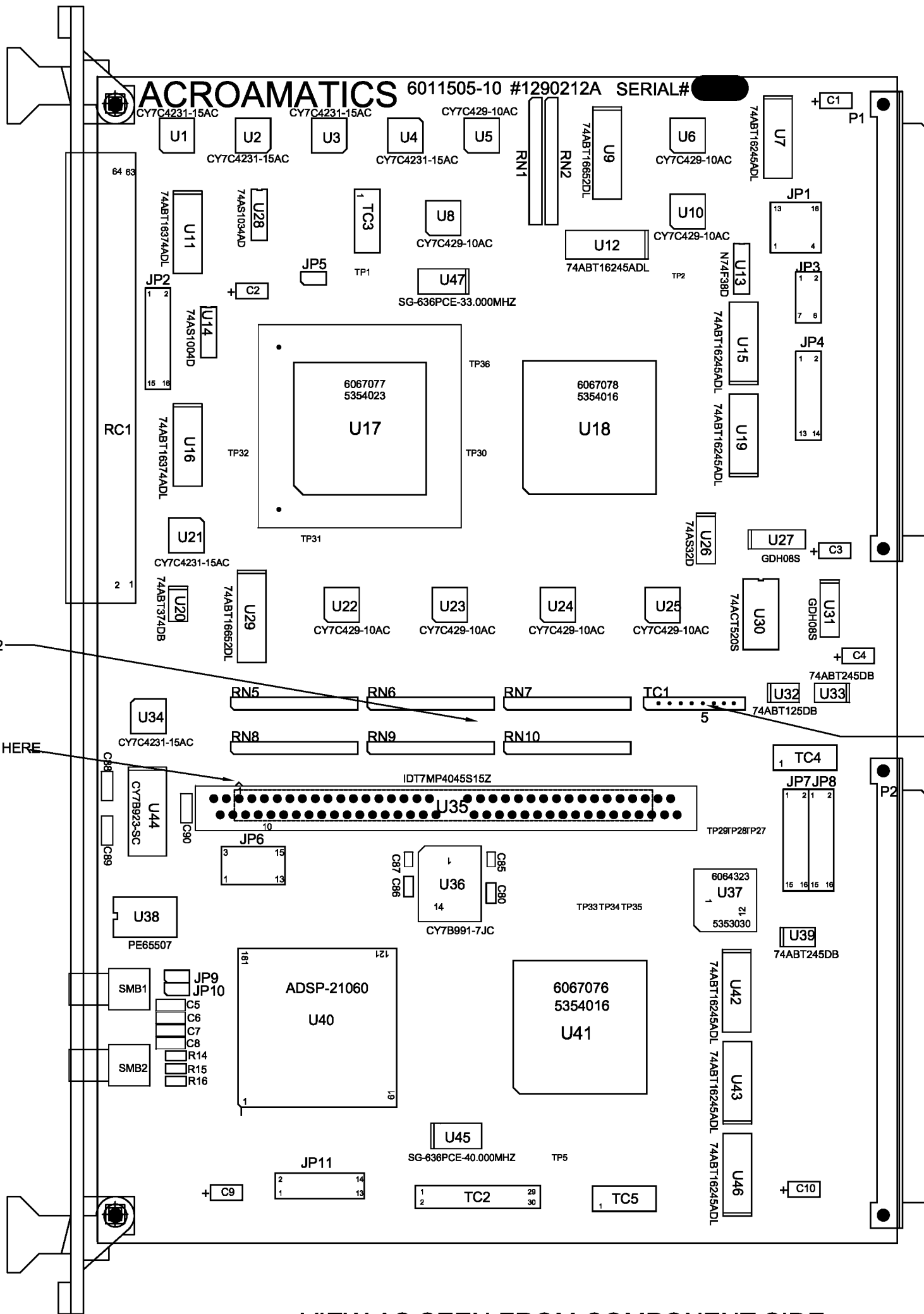
ASSEMBLY PN 6011505-10

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NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
42	6031096-01	1	ZIP SRAM 1MX32 17ns	CYM1851PZ-17C	CYPRESS	U35
43	6350054	1	OSCIL. XTAL 40.000MHZ SMT	SG-636PCE-40.000MC	EPSON	U45
44	6350055	1	OSCIL. XTAL 33.000MHZ SMT	SG-636PCE-33.000MC	EPSON	U47
45	9543006	1	XFMR DUAL FIBRE CHNL 266MHZ	PE65507	PULSE	U38
46	5353031	1	IC (ISP) GAL 22V10 7ns PLCC	ISPGAL22V10B-7LJ	LATTICE	U37, Program after installation
47	5354016	2	FPGA 16000 M-GATE PQFP	A42MX16-PQ160	ACTEL	Unprogrammed FPGA
48	5354029	1	FPGA 36000 GATE 208P PQFP	A42MX36-1PQ208	ACTEL	Unprogrammed FPGA
49						
50	6064323	1	PDSP CLOCK/WAIT	5353031-REV.A	ACROAMATICS	U37 ITEM 46
51	6067076	1	VME SHRC DISTRIBUTION INTF	5354016-REV.E	ACROAMATICS	U41, PDSP7076 ITEM 47
52	6067077	1	VME SHRC ABUS INTERFACE	5354023-REV.E	ACROAMATICS	U17, PDSP7077 ITEM 48
53	6067078	1	VME SHRC VME INTERFACE	5354016-REV.A	ACROAMATICS	U18, PDSP7078 ITEM 47
54						
55	9070015	2	DIP SWITCH 8-POS SLIDE SMT	GDH08S	AUGAT	U27,U31
56	5470011	1	JUMPER PINS SINGLE ROW 50POS	MTSW-150-07-G-S-24	SAMTEC	TC1(8 pins),TP1,TP2,TP5 TP27,TP28,TP29
56						
57	5470012	2	JUMPER PINS DOUBLE ROW 50POS	MTSW-150-07-G-D-24	SAMTEC	JP1(16 pins),JP2(16 pins) JP3(8 pins),JP4(14 pins) JP5(2 pins),JP6(15 pins) JP7(16 pins),JP8(16 pins) JP9(2 pins),JP10(2 pins) JP11(14 pins)
57						
57						
57						
57						
57						
58						
59	5600012	1	LABEL,VME PNL, ACRO	5600012	ACROAMATICS	
60	5600018	1	LABEL,VME PNL, PDSP	5600018	ACROAMATICS	
61	6730092	1	FR PNL-VME BLANK	6U4EF0000	TRIPLE-E	SCRN #8071194, MOD #5951132



NOTE 1
INSTALL PIN 1 HERE

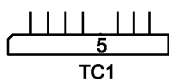
NOTE 2

NOTE 4

VIEW AS SEEN FROM COMPONENT SIDE

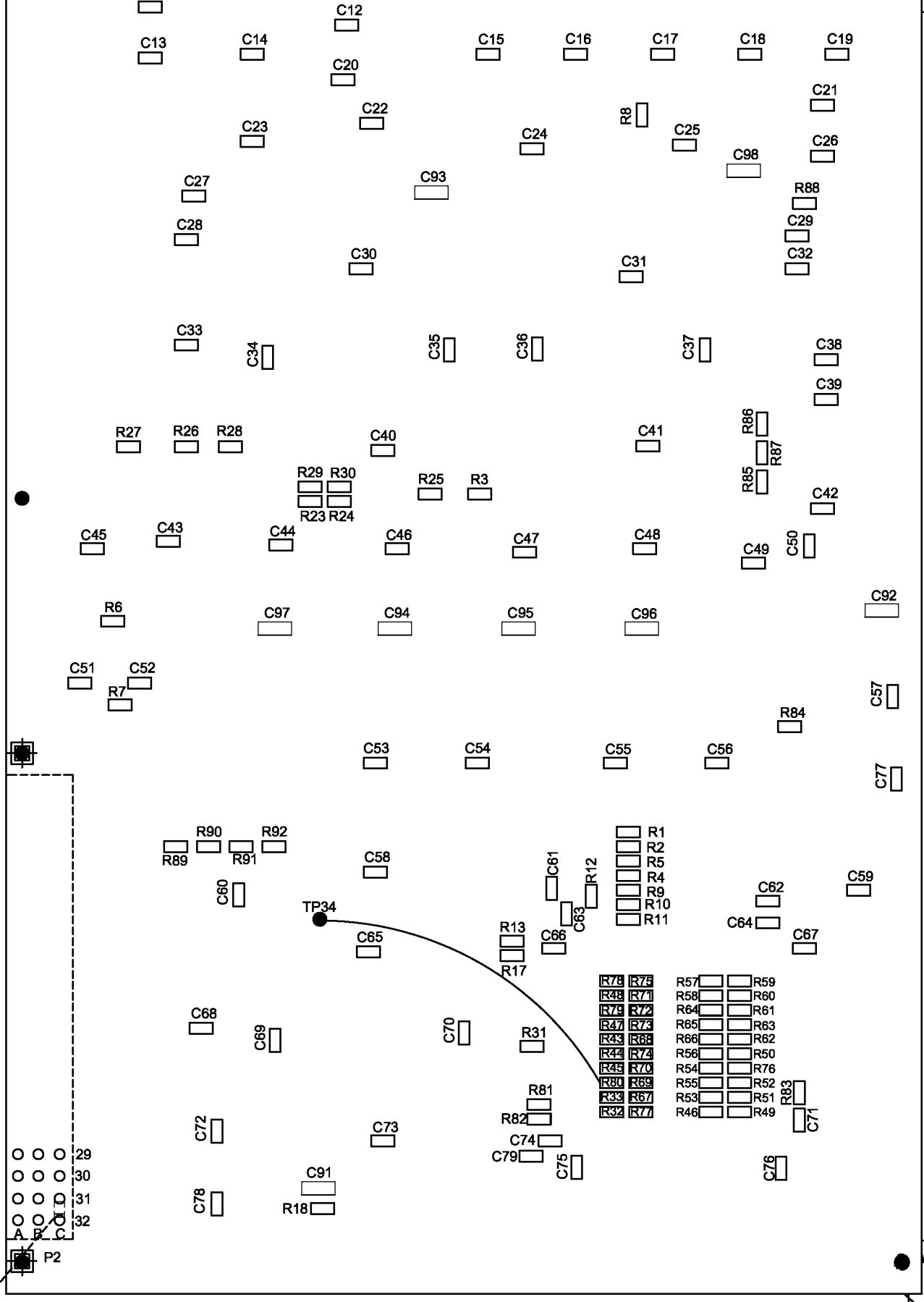
NOTES:

1. ALIGN MEMORY WITH CENTER HOLES OF U35.
2. ALIGN PIN 1 OF SIP RESISTORS (RN6, RN7, RN9, RN10) WITH PAD 1 AT LOCATIONS (RN6, RN7, RN9, RN10). LEAVE PAD 10 UNUSED.
3. INSTALL TEST POINTS (TP1, TP2, TP5, TP27, TP28, TP29) ONLY. LEAVE ALL OTHER TEST POINT LOCATION EMPTY.
4. CUT PIN 5 OF TC1 AS SHOWN IN DRAWING.



DR	B. GALAZIOS	2/04	ACROAMATICS <small>TELEMETRY SYSTEMS</small> GOLETA, CAL. 93117		
CHK					
A P P D			ASSEMBLY, CIRCUIT CARD PROGRAMMABLE DATA STREAM PROCESSOR		
NEXT ASSY	USED ON	SIZE	SCALE	DWG NO.	
		B	NTS	6011505-11	
APPLICATION		SHEET	2 OF 3		REV L

SERIAL# #1290212A 6011505-10 ACROAMATICS



VIEW AS SEEN THROUGH COMPONENT SIDE

SOLDER D1 ON TOP OF PINS C32 & C31 OF P2 CONNECTOR
MAKE SURE THE CATHODE IS ON C32 PIN

NOTE: SOLDER WIRE FROM TP34 TO R80 AS SHOWN ABOVE

DR	B. GALAZIOS	2/04	ACROAMATICS <small>TELEMETRY SYSTEMS GOLETA, CAL. 93117</small>		
CHK			ASSEMBLY, CIRCUIT CARD PROGRAMMABLE DATA STREAM PROCESSOR		
A			SIZE	SCALE	DWG NO.
P			B	NTS	6011505-11
D			NEXT ASSY	USED ON	
APPLICATION			SHEET	3 OF 3	REV L

**LIST OF MATERIALS
VME PDSP (1MB)**

8111505-11

PAGE 1 OF 2

ASSEMBLY PN 6011505-11

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ENGINEERING APPROVAL _____ DATE _____

MANUFACTURING APPROVAL _____ DATE _____

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
1	1290212	1	PCB VME PDSP	1290212	ACROAMATICS	
2	2796061	2	CONN PC 96P SDR RTANGL	7296-50C2TH	3M	P1,P2
3	2796060	1	CONN PC 64P SDR RTANGL	2564-5002UB	3M	RC1
4	2796057	2	CONN PC SMB RTANGLE 1P	903-373J-51A	AMPHENOL	SMB1,SMB2
5	2796101	1	CONN PC 30 PIN HEADER SMT	DF13-30DP-1.25	HIROSE	TC2
6	2796104	3	CONN PC 7PIN 1.25 HEADER SMT	53398-0790	MOLEX	TC3,TC4,TC5
7						
8						
9	3573821	1	DIODE SCHOTTKY SMT 200mA	MA2SD10CT-ND	PANASONIC	D1
10						
11	1903063	11	CAP TMP STBL (X7R) .022uF SMT	ECU-V1H223KBM	PANASONIC	C88-C98
12	1903069	71	CAP X7R .1uF 5% 50V SMT-805	C0805C104J5RAC	KEMET	C11-C80,C86
13	1922643	6	CAP TA 10uF 10% 16V SMT	T491B106016AS	KEMET	C1-C4,C9,C10
13			Acceptable substitute is:	ECS-T1CX106R	PANASONIC	
14	1904101	4	CAP NPO 1000pF 50V SMT 1206	ECU-V1H102JCH	PANASONIC	C5-C8
15	1904106	2	CAP NPO 100pF 5% 50V SMT	ECU-V1H101JCV	PANASONIC	C85,C87
16						
17	7680974	5	RES 121 OHM .1W 1% SMT-0805	ERJ-6ENF121	PANASONIC	R2,R5,R10,R12,R13
18	7680975	5	RES 39.2 OHM .1W 1% SMT-0805	ERJ-6ENF39.2	PANASONIC	R1,R4,R9,R11,R17
19	7680979	27	RES 1K .1W 1% SMT-0805	ERJ-6ENF1.00K	PANASONIC	R6,R31,R45-R69
20	7680980	3	RES 33.2 OHM .1W 1% SMT-0805	ERJ-6ENF33.2	PANASONIC	R85,R86,R87
21	7680981	35	RES 10K .1W 1% SMT-0805	ERJ-6ENF10.0K	PANASONIC	R7,R8,R18,R23-R30,R32,R33 R43,R44,R70-R84,R88-R92
21						
22	7680988	4	RES 267 OHM .1W 1% SMT-0805	ERJ-6ENF267	PANASONIC	R3,R14,R15,R16
23						
24	7700036	4	RES SIP 1.5K/3.3K 10P 2%	CSC10A05-152/332-G	DALE	RN1,RN2,RN5,RN8
25	7700055	4	RES SIP 1K 8R 9P LOW PROFILE	CSC09A-01-102G	DALE	RN6,RN7,RN9,RN10
26	5300004-42	1	IC HEX INVERTER (SMD)	74AS1004D	GENERIC	U14
27	5300034-37	1	IC HEX DRIVER +-48ma SMT	74AS1034AD	GENERIC	U28
28	5300038-39	1	IC QUAD 2-INP NAND BUFF(SMD)	N74F38D	GENERIC	U13
29	5300032-91	1	IC QUAD 2-INP OR GATE SMT	74AS32D	GENERIC	U26
30	5300125-49	1	IC QUAD BUF NI INDEP-TS SMT	74ABT125DB	GENERIC	U32
31	5300245-55	7	IC 16BIT BUS XCVR SMT NI TS	74ABT16245ADL	GENERIC	U7,U12,U15,U19,U42,U43,U46
32	5300245-91	2	IC OCT BUS XCVR NI TS SMT	74ABT245DB	GENERIC	U33,U39
33	5300374-55	2	IC 16BIT D-F/F EDGE-TRIG SMT	74ABT16374ADL	GENERIC	U16,U11
34	5300374-91	1	IC OCT D-F/F EDGE-TRIG SMT	74ABT374DB	TI	U20
34			Acceptable substitute is:	74ABT374CMSA	NATIONAL	
35	5300520-63	1	IC 8-BIT MAG COMP SMT	74ACT520S	NATIONAL	U30
36	5300652-55	2	IC 16BIT BUS XCVR W/RGSTRS TS	74ABT16652DL	GENERIC	U9,U29
37	5308003	1	IC 160-330MBPS SERIAL XMIT	CY7B923-SC	CYPRESS	U44
38	5308991	1	IC PROGRAMMABLE SKEW CLK BUF	CY7B991-7JC	CYPRESS	U36
39	5308429-10	8	IC 2Kx9-BIT FIFO (QFP)	CY7C429-10AC	CYPRESS	U5,U6,U8,U10,U22-U25
40	5308423-15	6	IC 2Kx9 SYNCHRONOUS FIFO SMT	CY7C4231-15AC	CYPRESS	U1,U2,U3,U4,U21,U34
40			Acceptable substitute is:	IDT72231L15PF	IDT	
41	6128060	1	IC 32-BIT DSP COMPUTER 40M	ADSP-21060KS-160	ANALOG-DEVICE	U40

**LIST OF MATERIALS
VME PDSP (1MB)**

8111505-11

PAGE 2 OF 2

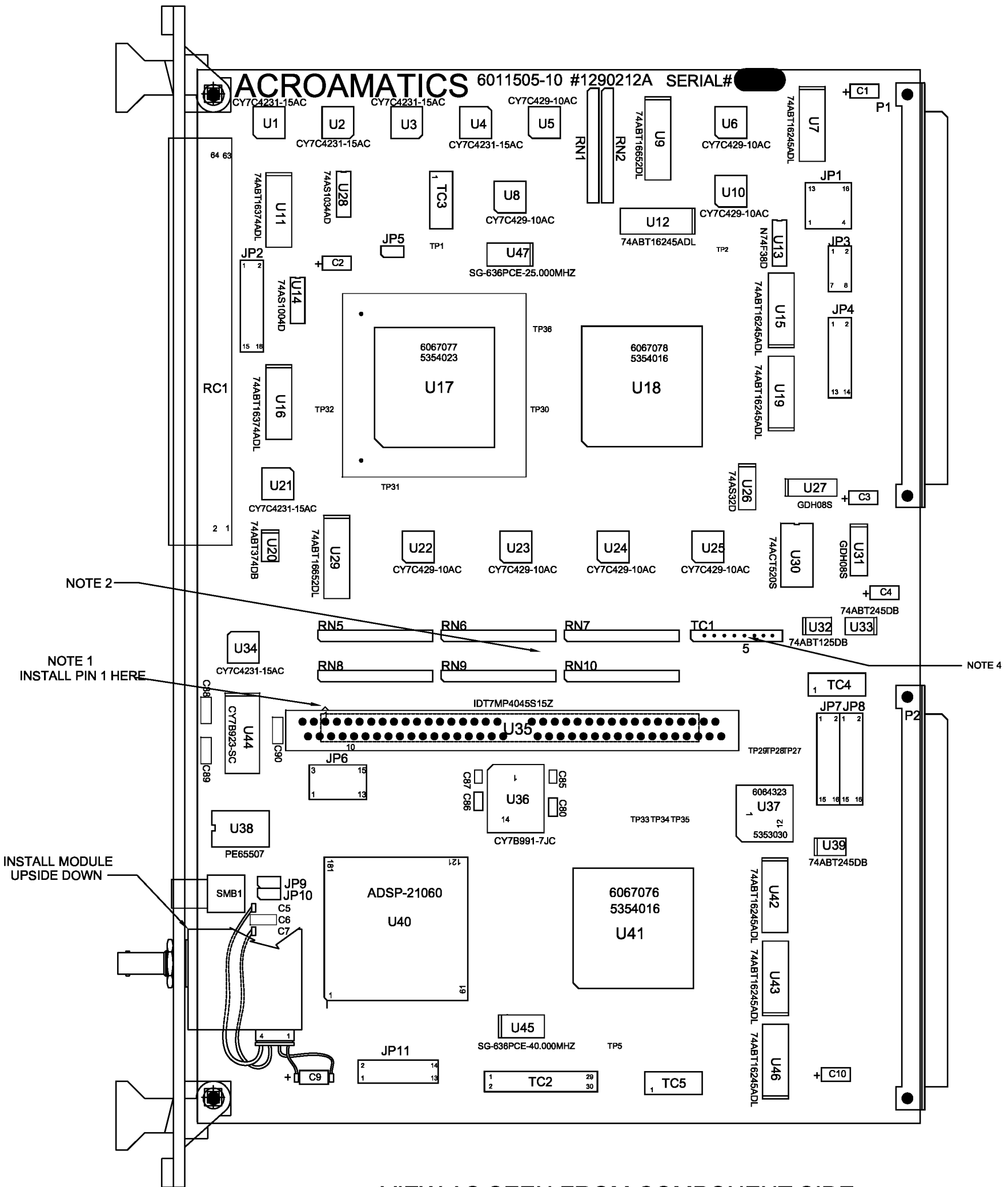
ASSEMBLY PN 6011505-11

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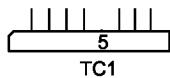
NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
42	6031116	1	ZIP SRAM 256KX32 15ns	CYM1841BPZ-15C	CYPRESS	U35
42			Acceptable substitute is:	IDT7MP4045S15Z	IDT	
42			Acceptable substitute is:	CYM1841APZ-15C	CYPRESS	
42			Acceptable substitute is:	MCM32257Z15	MOTOROLA	
43	6350054	1	OSCIL. XTAL 40.000MHZ SMT	SG-636PCE-40.000MC	EPSON	U45
44	6350055	1	OSCIL. XTAL 33.000MHZ SMT	SG-636PCE-33.000MC	EPSON	U47
45	9543006	1	XFMR DUAL FIBRE CHNL 266MHZ	PE65507	PULSE	U38
46	5353031	1	IC (ISP) GAL 22V10 7ns PLCC	ISPGAL22V10B-7LJ	LATTICE	U37, Program after installation
47	5354016	2	FPGA 16000 M-GATE PQFP	A42MX16-PQ160	ACTEL	Unprogrammed FPGA
48	5354029	1	FPGA 36000 GATE 208P PQFP	A42MX36-1PQ208	ACTEL	Unprogrammed FPGA
49						
50	6064323	1	PDSP CLOCK/WAIT	5353031-REV.A	ACROAMATICS	U37 ITEM 46
51	6067076	1	VME SHRC DISTRIBUTION INTF	5354016-REV.E	ACROAMATICS	U41, PDSP7076 ITEM 47
52	6067077	1	VME SHRC ABUS INTERFACE	5354023-REV.E	ACROAMATICS	U17, PDSP7077 ITEM 48
53	6067078	1	VME SHRC VME INTERFACE	5354016-REV.A	ACROAMATICS	U18, PDSP7078 ITEM 47
54						
55	9070015	2	DIP SWITCH 8-POS SLIDE SMT	GDH08S	AUGAT	U27,U31
56	5470011	1	JUMPER PINS SINGLE ROW 50POS	MTSW-150-07-G-S-24	SAMTEC	TC1(8 pins),TP1,TP2,TP5 TP27,TP28,TP29
56						
57	5470012	2	JUMPER PINS DOUBLE ROW 50POS	MTSW-150-07-G-D-24	SAMTEC	JP1(16 pins),JP2(16 pins) JP3(8 pins),JP4(14 pins) JP5(2 pins),JP6(15 pins) JP7(16 pins),JP8(16 pins) JP9(2 pins),JP10(2 pins) JP11(14 pins)
57						
57						
57						
57						
57						
58						
59	5600012	1	LABEL,VME PNL, ACRO	5600012	ACROAMATICS	
60	5600018	1	LABEL,VME PNL, PDSP	5600018	ACROAMATICS	
61	6730092	1	FR PNL-VME BLANK	6U4EF0000	TRIPLE-E	SCRN #8071194, MOD #5951132



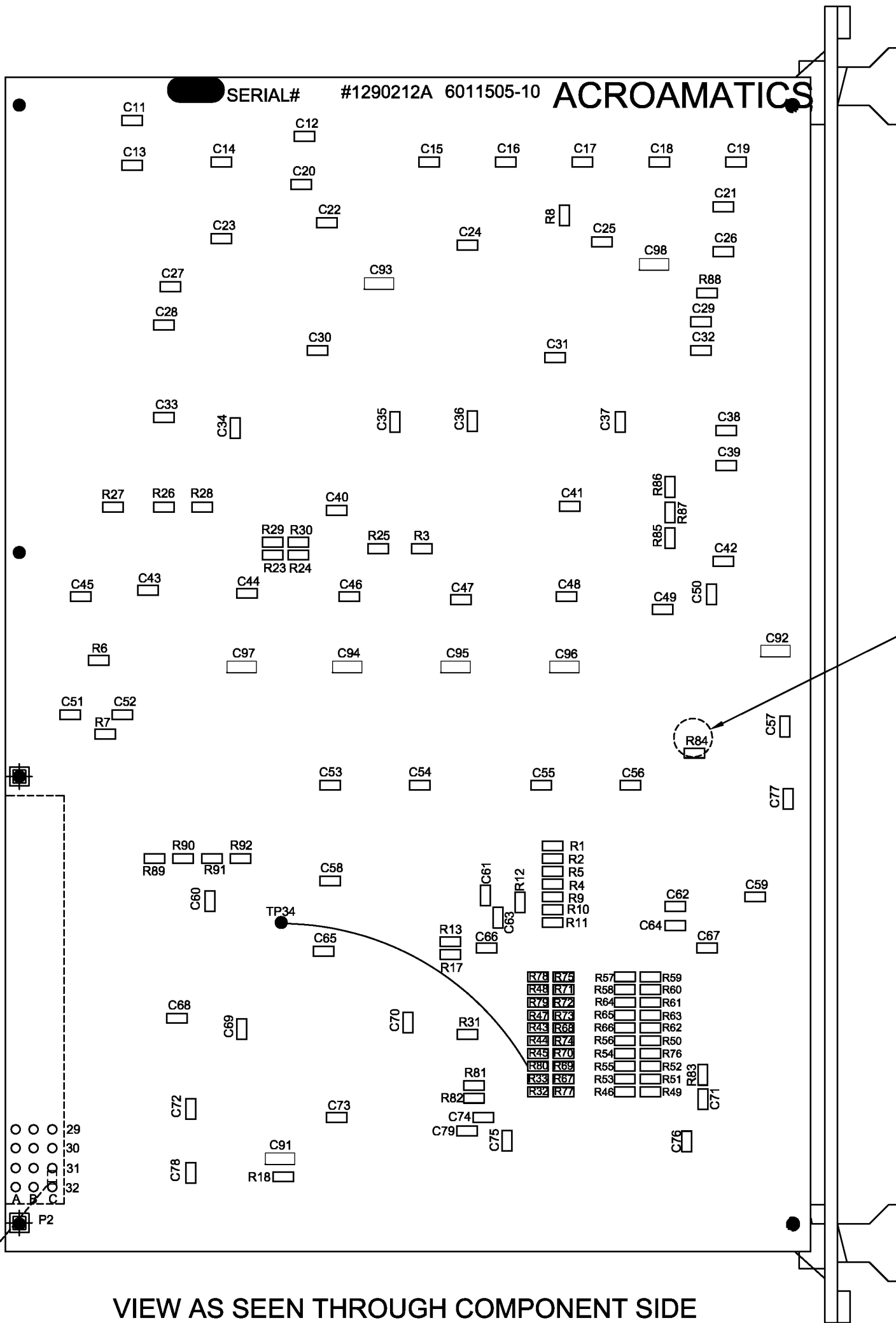
VIEW AS SEEN FROM COMPONENT SIDE

NOTES:

1. ALIGN MEMORY WITH CENTER HOLES OF U35.
2. ALIGN PIN 1 OF SIP RESISTORS (RN6, RN7, RN9, RN10) WITH PAD 1 AT LOCATIONS (RN6, RN7, RN9, RN10). LEAVE PAD 10 UNUSED.
3. INSTALL TEST POINTS (TP1, TP2, TP5, TP27, TP28, TP29) ONLY. LEAVE ALL OTHER TEST POINT LOCATION EMPTY.
4. CUT PIN 5 OF TC1 AS SHOWN IN DRAWING.



DR	D MACDONALD	10/04	ACROAMATICS <small>TELEMETRY SYSTEMS</small> GOLETA, CAL. 93117		
CHK					
A P P D			ASSEMBLY, CIRCUIT CARD PROGRAMMABLE DATA STREAM PROCESSOR with OPTICAL LINK		
			SIZE	SCALE	DWG NO.
			B	NTS	6011505-12
	NEXT ASSY	USED ON	SHEET	2 OF 3	REV A
	APPLICATION				



VIEW AS SEEN THROUGH COMPONENT SIDE

SOLDER D1 ON TOP OF PINS C32 & C31 OF P2 CONNECTOR
MAKE SURE THE CATHODE IS ON C32 PIN

NOTE: SOLDER WIRE FROM TP34 TO R80 AS SHOWN ABOVE

DR	D MACDONALD	10/04	ACROAMATICS <small>TELEMETRY SYSTEMS GOLETA, CAL. 93117</small>		
CHK			ASSEMBLY, CIRCUIT CARD PROGRAMMABLE DATA STREAM PROCESSOR with OPTICAL LINK		
A P P D			SIZE B	SCALE NTS	DWG NO. 6011505-12
	NEXT ASSY	USED ON	SHEET	3 OF 3	REV A
APPLICATION					

**LIST OF MATERIALS
VME PDSP (OPTICAL LINK)**

8111505-12

PAGE 1 OF 2

ASSEMBLY PN 6011505-12

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REVISION A

ENGINEERING APPROVAL _____ DATE _____

MANUFACTURING APPROVAL _____ DATE _____

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
1	1290212	1	PCB VME PDSP	1290212	ACROAMATICS	
2	2796061	2	CONN PC 96P SDR RTANGL	7296-50C2TH	3M	P1,P2
3	2796060	1	CONN PC 64P SDR RTANGL	2564-5002UB	3M	RC1
4	2796057	1	CONN PC SMB RTANGLE 1P	903-373J-51A	AMPHENOL	SMB1
5	2796101	1	CONN PC 30 PIN HEADER SMT	DF13-30DP-1.25	HIROSE	TC2
6	2796104	3	CONN PC 7PIN 1.25 HEADER SMT	53398-0790	MOLEX	TC3,TC4,TC5
7						
8						
9	3573821	1	DIODE SCHOTTKY SMT 200mA	MA2SD10	PANASONIC	D1
10						
11	1903063	11	CAP TMP STBL (X7R) .022uF SMT	ECU-V1H223KBM	PANASONIC	C88-C98
12	1903069	71	CAP X7R .1uF 5% 50V SMT-805	C0805C104J5RAC	KEMET	C11-C80,C86
13	1922643	6	CAP TA 10uF 10% 16V SMT	T491B106016AS	KEMET	C1-C4,C9,C10
13			Acceptable substitute is:	ECS-T1CX106R	PANASONIC	
14	1904101	2	CAP NPO 1000pF 50V SMT 1206	ECU-V1H102JCH	PANASONIC	C6,C8
15	1904106	2	CAP NPO 100pF 5% 50V SMT	ECU-V1H101JCV	PANASONIC	C85,C87
16						
17	7680974	5	RES 121 OHM .1W 1% SMT-0805	ERJ-6ENF121	PANASONIC	R2,R5,R10,R12,R13
18	7680975	5	RES 39.2 OHM .1W 1% SMT-0805	ERJ-6ENF39.2	PANASONIC	R1,R4,R9,R11,R17
19	7680979	27	RES 1K .1W 1% SMT-0805	ERJ-6ENF1.00K	PANASONIC	R6,R31,R45-R69
20	7680980	3	RES 33.2 OHM .1W 1% SMT-0805	ERJ-6ENF33.2	PANASONIC	R85,R86,R87
21	7680981	35	RES 10K .1W 1% SMT-0805	ERJ-6ENF10.0K	PANASONIC	R7,R8,R18,R23-R30,R32,R33 R43,R44,R70-R84,R88-R92
21						
22	7680988	2	RES 267 OHM .1W 1% SMT-0805	ERJ-6ENF267	PANASONIC	R14,R15
23						
24	7700036	4	RES SIP 1.5K/3.3K 10P 2%	CSC10A05-152/332-G	DALE	RN1,RN2,RN5,RN8
25	7700055	4	RES SIP 1K 8R 9P LOW PROFILE	CSC09A-01-102G	DALE	RN6,RN7,RN9,RN10
26	5300004-42	1	IC HEX INVERTER (SMD)	74AS1004D	GENERIC	U14
27	5300034-37	1	IC HEX DRIVER +-48ma SMT	74AS1034AD	GENERIC	U28
28	5300038-39	1	IC QUAD 2-INP NAND BUFF(SMD)	N74F38D	GENERIC	U13
29	5300032-91	1	IC QUAD 2-INP OR GATE SMT	74AS32D	GENERIC	U26
30	5300125-49	1	IC QUAD BUF NI INDEP-TS SMT	74ABT125DB	GENERIC	U32
31	5300245-55	7	IC 16BIT BUS XCVR SMT NI TS	74ABT16245ADL	GENERIC	U7,U12,U15,U19,U42,U43,U46
32	5300245-91	2	IC OCT BUS XCVR NI TS SMT	74ABT245DB	GENERIC	U33,U39
33	5300374-55	2	IC 16BIT D-F/F EDGE-TRIG SMT	74ABT16374ADL	GENERIC	U16,U11
34	5300374-91	1	IC OCT D-F/F EDGE-TRIG SMT	74ABT374DB	TI	U20
34			Acceptable substitute is:	74ABT374CMSA	NATIONAL	
35	5300520-63	1	IC 8-BIT MAG COMP SMT	74ACT520S	NATIONAL	U30
36	5300652-55	2	IC 16BIT BUS XCVR W/RGSTRS TS	74ABT16652DL	GENERIC	U9,U29
37	5308003	1	IC 160-330MBPS SERIAL XMIT	CY7B923-SC	CYPRESS	U44
38	5308991	1	IC PROGRAMMABLE SKEW CLK BUF	CY7B991-7JC	CYPRESS	U36
39	5308429-10	8	IC 2Kx9-BIT FIFO (QFP)	CY7C429-10AC	CYPRESS	U5,U6,U8,U10,U22-U25
40	5308423-15	6	IC 2Kx9 SYNCHRONOUS FIFO SMT	CY7C4231-15AC	CYPRESS	U1,U2,U3,U4,U21,U34
40			Acceptable substitute is:	IDT72231L15PF	IDT	
41	6128060	1	IC 32-BIT DSP COMPUTER 40M	ADSP-21060KS-160	ANALOG-DEVICE	U40

**LIST OF MATERIALS
VME PDSP (OPTICAL LINK)**

8111505-12

PAGE 2 OF 2

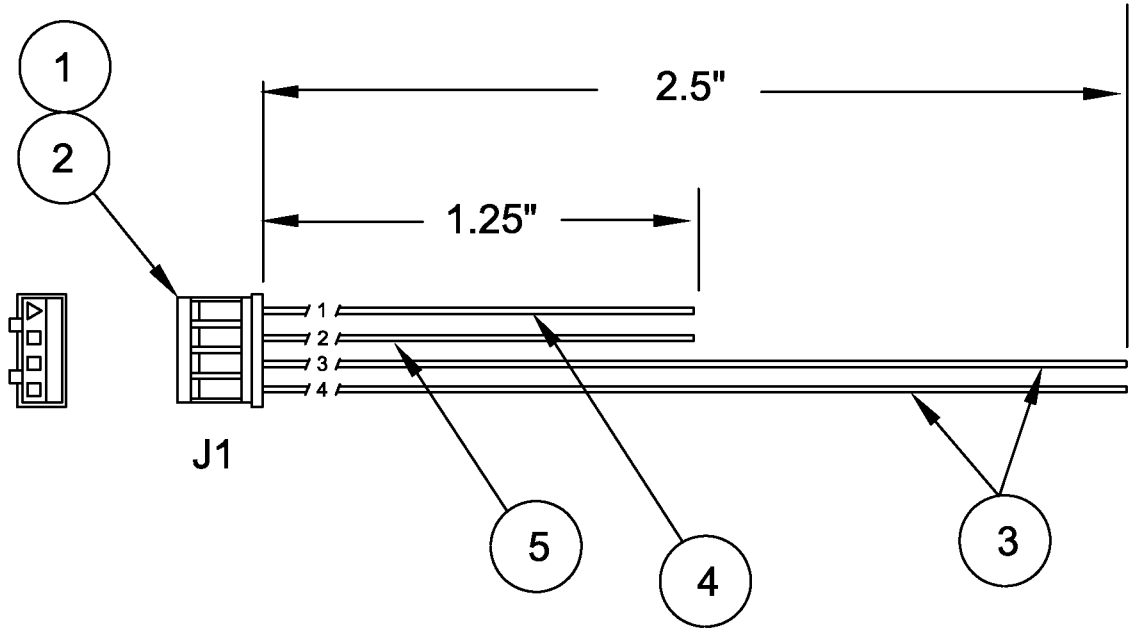
ASSEMBLY PN 6011505-12

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REVISION A

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
42	6031116	1	ZIP SRAM 256KX32 15ns	CYM1841BPZ-15C	CYPRESS	U35
42			Acceptable substitute is:	IDT7MP4045S15Z	IDT	
42			Acceptable substitute is:	CYM1841APZ-15C	CYPRESS	
42			Acceptable substitute is:	MCM32257Z15	MOTOROLA	
43	6350054	1	OSCIL. XTAL 40.000MHZ SMT	SG-636PCE-40.000MC	EPSON	U45
44	6350063	1	OSCIL. XTAL 25.000MHZ SMT 3V	SG-636PCE-25.000	EPSON	U47
45	9543006	1	XFMR DUAL FIBRE CHNL 266MHZ	PE65507	PULSE	U38
46	5353031	1	IC (ISP) GAL 22V10 7ns PLCC	ISPGAL22V10B-7LJ	LATTICE	U37, Program after installation
47	5354016	2	FPGA 16000 M-GATE PQFP	A42MX16-PQ160	ACTEL	Unprogrammed FPGA
48	5354029	1	FPGA 36000 GATE 208P PQFP	A42MX36-1PQ208	ACTEL	Unprogrammed FPGA
49						
50	6064323	1	PDSP CLOCK/WAIT	5353031-REV.A	ACROAMATICS	U37 ITEM 46
51	6067076	1	VME SHRC DISTRIBUTION INTF	5354016-REV.E	ACROAMATICS	U41, PDSP7076 ITEM 47
52	6067077	1	VME SHRC ABUS INTERFACE	5354023-REV.E	ACROAMATICS	U17, PDSP7077 ITEM 48
53	6067078	1	VME SHRC VME INTERFACE	5354016-REV.A	ACROAMATICS	U18, PDSP7078 ITEM 47
54						
55	9070015	2	DIP SWITCH 8-POS SLIDE SMT	GDH08S	AUGAT	U27,U31
56	5470011	1	JUMPER PINS SINGLE ROW 50POS	MTSW-150-07-G-S-24	SAMTEC	TC1(8 pins),TP1,TP2,TP5 TP27,TP28,TP29
56						
57	5470012	2	JUMPER PINS DOUBLE ROW 50POS	MTSW-150-07-G-D-24	SAMTEC	JP1(16 pins),JP2(16 pins) JP3(8 pins),JP4(14 pins) JP5(2 pins),JP6(15 pins) JP7(16 pins),JP8(16 pins) JP9(2 pins),JP10(2 pins) JP11(14 pins)
57						
57						
57						
57						
58	6051259	1	OPTICAL HOTLINK TRANSMITTER	6051259	ACROAMATICS	
59	1716543	1	CBL 4 PIN TO SOLDER TAIL	1716543	ACROAMATICS	
60	5600012	1	LABEL,VME PNL, ACRO	5600012	ACROAMATICS	
61	5600018	1	LABEL,VME PNL, PDSP	5600018	ACROAMATICS	
62	6730092	1	FR PNL-VME BLANK	6U4EF0000	TRIPLE-E	SCRN #8071194, MOD #5951132



USED ON	DRAWN BY	ACROAMATICS INC.		
	D MACDONALD	CABLE DRAWING		
	DATE	TITLE		
	10/04	FIBER OPTIC MODULE		
	CHECKED BY	CABLE ADAPTER - 4 PIN		
	DATE	SIZE	DRAWING #	REV.
	APPROVED BY	A	1716543	A
	DATE	SCALE	SHEET	
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**LIST OF MATERIALS
CBL OPTICAL HOTLINK**

8176543

PAGE 1 OF 1

ASSEMBLY PN 1716543

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REVISION A

ENGINEERING APPROVAL _____ DATE _____

MANUFACTURING APPROVAL _____ DATE _____

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
1	2794219	1	CONN HOUSING 4 POS 2mm	DF3-4S-2C	HIROSE	P03
2	2796154	4	CONN SCKT 24-28 AWG CRIMP GLD	DF3-2428SCFC	HIROSE	
3	9800102	2	WIRE 26 AWG TEF WHITE	EXE1938-26-9	MIL-SPEC	2 1/2" long
4	9800231	1	WIRE 24 AWG RED	1550	ALPHA	1 1/4" long
5	9800271	1	WIRE 24 AWG BLACK	BU-1936-24-0	MIL-SPEC	1 1/4" long