DN 6000368

TECHNICAL MANUAL
MODEL 482M MEZZANINE
DAC / ADC CARD

Acroamatics, Inc.
70 South Kellogg Avenue
Goleta, CA 93117-3476

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ACROAMATICS DOCUMENT HISTORY

The following table indicates major changes made to *Technical Manual - Model 480 DAC/ADC Converter*, Acroamatics Document Number 6000368, released on November 26, 2001, and contains a record of all revisions made since that date.

DN6000368 CHANGE HISTORY			
Rev	**Date**	**Action**	**Name**
	11-26-01	Original Issue	DJM
	10-01-02	JF cable clarifications	DJM

TECHNICAL MANUAL
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TECHNICAL MANUAL
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SECTION 1
INTRODUCTION

1.1 DESCRIPTION

The 482M (DAC/ADC mezzanine card) plugs on to the Acroamatics 1605P PDSP (Programmable Data Stream Processor) PCI card to add the following features:

1) 32 Analog and 32 Discrete lines

2) A 16 channel Analog to Digital Converter

3) A Fiber-optic, high-speed serial External DAC Bus

These additional features are available in the dash-number combinations described on the next page. The mezzanine connector contains a 16-bit interface to the local bus, which allows the host computer to setup and control mezzanine functions.

The mezzanine connector also provides access to the 32-bit A-bus. The analog to digital converter uses the A-bus to transfer messages to the PDSP card by creating messages to the Feedback Port (Device 4) which are processed just like messages received from the I-bus.

You access the digital to analog converters and discrete line registers by sending A-bus messages to Device 7 (the DAC Bus). The address portion of the message is compared to the address assigned to the 482M card and (if they match the current message) the channel address, control bits, and data word are captured and processed as a DAC channel or a discrete line as defined by the control bits. All messages to Device 7 are also captured as 32-bit messages, serialized, and transmitted over a high speed, fiber optical *Serial DAC Bus Output.* This fiber optical output allows external DAC chassis to be located several hundred feet from the TDP chassis, and also allows you to expand your system DAC/Discrete line complement to a maximum of 4096 analog and 4096 discrete outputs.

The 16 channel analog to digital converter accepts differential signals up to +/- 5 Volts full scale with 12-bit resolution. Each channel has individually programmable sampling rate ranges of 32 to 400,000 samples per second. You can also create a single high rate channel by connecting the input signal to an input pair, i.e. channels 0 & 1, and selecting the same sampling rate for the two channels with a *skewed* sampling interval. This provides a single output at up to 800,000 samples per second.

1.2 CARD VERSIONS

The 482M card comes in three versions:

Part number 6011482-11 provides 32 analog and 32 discrete output lines, a 16 channel Analog to Digital converter, and a HOTLink™ fiber-optic external DAC bus. This version of the card is supplied with two adapter cables (PN 1716422). These cables adapt the mezzanine ribbon cable connectors at one end to 68 pin connectors, mounted on rear panel fingers, at the other. Installing the fingers at two unused PCI or ISA slot provides convenient external access.

The 482M-32 (part number 6011482-12) is the same as the 6011482-11 above, but without the HOTLink™ circuit.

The 482M-8 (part number 6011482-13) is a simplified configuration providing eight analog and sixteen discrete lines only, and does not include A to D conversion, the fiber-optic external DAC bus, or any cables.

1.3 DOCUMENT CONVENTIONS

In this document register addresses and address offsets are hexadecimal numbers. Where it is necessary to refer to a hexadecimal number in the text, we use the C programming convention *0xNN* to refer to hexadecimal number *NN*. Bits in a register are numbered in decimal. The term *Device n* refers to an address destination on the TDP system A-Bus. The A-bus is the output data bus, and has eight possible destination devices. Although we do not use all eight, those destinations we do use are dedicated to specific functions in the TDP system. The term *DIT* refers to a data message in the TDP system. It stands for “Data, ID, and Time,” the three components of a TDP data message. We can label a DIT by the value of its ID tag, for example “DIT 0xFFF1,” the DIT that conveys the once per millisecond value of a time message. Frequently we use a functional label instead, for example, *the MILLISECOND DIT.*

SPECIFICATIONS - MODEL 482M MEZZANINE CARD
DAC & ADC CONVERTERS

FUNCTION	CHARACTERISTICS
Input Setup Bus & connections to the A-bus	Interfaces to Acroamatics 1605 PDSP over a mezzanine connector *OPTIONAL: Optical serial bus connection
ANALOG OUTPUT	Output loaded with 10kOhm and 50pf in parallel
Resolution	12 bits of resolution, 2's complement binary input
Accuracy	±2 LSB
Linearity	±1 LSB
Stability	10ppm/°C
Settling Time	2.5 ∝sec to within ±1 LSB
Slew Rate	3 Volts/∝secs
Output Current	1 mA maximum @±5V
Output Voltage	–5V to +5V
DISCRETE OUTPUT	
Outputs	32 discrete output lines are TTL Compatible.
Addressing Modes	The discrete outputs may be addressed as two 16-bit registers, four 8-bit registers, or 32 1-bit registers. When selected as 16-bit registers, you can use strobe and acknowledge signals to synchronize message transfers
Output current	-32ma @2.4V, and 48ma @ 0.40V
ANALOG INPUT	**CHARACTERISTICS**
Differential	Sixteen inputs with individual instrumentation amplifiers.
Impedance	100k Ohms minimum
Input Amplitude	±5 Volts full scale
OPERATION	
Sampling Rate	32 to 800,000 samples per second
Resolution	12 bits
Data Format	Offset binary or twos complement, right or left justified
Nonlinearity	±1 LSB
Accuracy	±1 LSB
REQUIREMENTS	
Power	+5VDC at 2 Amperes ±12 Volts at 200 milliamperes
Temperature	Operating: 0 to +40°C, Non-operating: –40 to +86°C
Relative Humidity	Up to 90% non-condensing
Air Flow	30 Linear FPM
Shock	Operating: 6G, Non-operating: 50G
Vibration	Operating: 0.5G, 5 to 2000 Hz, Non-operating: 1.2G 5 to 500 Hz

Specifications are subject to change without notice.

SECTION 2
INSTALLATION

2.1 GENERAL

This section contains installation information for the Acroamatics Model 482M DAC/ADC card. The basic card part number is 6011482.

2.2 UNPACKING

Using proper ESD-protection procedures, open the cardboard shipping container and remove the card from the anti-static bag. Retain the container, anti-static bag, and foam packaging material for use if you must return the card.

2.3 FACTORY RETURN

When you return a card to the factory for repair or modification, include as much information as possible describing the failure mode or the modification/update you want.

Pack the card for shipment by wrapping it in the anti-static bag. Place the card into the shipping container, protecting it with the foam packing, and secure the container with reinforced tape. Provide the name and phone number of a technical contact we can talk to regarding the card.

Call Acroamatics at (805) 967-9909 to get a RMA number before returning any equipment to the factory, and include the RMA number in any correspondence or shipments to Acroamatics.

2.4 INSTALLING

Mounting dimensions are shown in the assembly drawing in Section 6.

2.5 CONNECTORS

The following pages contain tables of information on all the connections into and out of the Model 482M.

TABLE 2-1
MATING CONNECTORS FOR MODEL 482M
VERSIONS 482M-32, & 482M-8 (REDUCED)

CONN	FUNCTION	MATING CONNECTOR
J01	Mezzanine	3M 61083-104000
RC1	D-to-A 00-15 & Discrete Lines 00-15 - External Out	PI 1200-068P-SCSI-III
RC2	D-to-A 16-31 & Discrete Lines 16-31 - External Out (Optional)	3M 82068-6006
RC3	Analog Inputs 00-15 (Optional)	3M 82068-6006
TC1	Test	MOLEX 51021-0700
U5	DAC Bus F/O (Optional)	F.O. ST 62/125

482M-8 (8 DACS/16 Discretes) does not provide RC2, RC3, and U5 outputs.

TABLE 2-2
EXTERNAL CABLES SUPPLIED WITH 482M-32
FOR ANALOG INPUTS, DAC, & LINES 16-31

DESCRIPTION	MEZZANINE CONNECTOR	
	RC2	**RC3**
DATA LINES	D to A Lines 16-31 & Discrete Lines 16-31	Analog Inputs 0-15
CABLE NUMBER	1716422	1716422
MATING CONN	PI 1200-068P-SCSI-III	PI 1200-068P-SCSI-III

These cables extend the signals on RC2 and RC3 through unused PCI or ISA slot connectors to provide convenient external access. See TABLE 2-9 for RC2 cable signal list, and TABLE 2-10 for RC3 cable signal list.

TABLE 2-3. CONNECTOR LIST
MODEL 482M CONNECTOR J01
MEZZANINE

PIN	SIGNAL	FUNCTION
01	VCC5	+5Vdc
02	GND	Ground
03	VCC5	+5Vdc
04	GND	Ground
05	9AWORD1	A-BUS Last Word Flag
06	4ADEST0	A-BUS Destination Select 0
07	4ADEST1	A-BUS Destination Select 1
08	4ADEST2	A-BUS Destination Select 2
09	GND	Ground
10	9AOWAIT	A-BUS Wait
11	9AOREST	A-BUS Reset
12	4AOUT0	A-BUS Bit 0
13	4AOUT1	A-BUS Bit 1
14	GND	Ground
15	4AOUT2	A-BUS Bit 2
16	4AOUT3	A-BUS Bit 3
17	4AOUT4	A-BUS Bit 4
18	4AOUT5	A-BUS Bit 5
19	GND	Ground
20	4AOUT6	A-BUS Bit 6
21	4AOUT7	A-BUS Bit 7
22	4AOUT8	A-BUS Bit 8
23	4AOUT9	A-BUS Bit 9
24	GND	Ground
25	4AOUT10	A-BUS Bit 10
26	4AOUT11	A-BUS Bit 11
27	4AOUT12	A-BUS Bit 12
28	4AOUT13	A-BUS Bit 13
29	GND	Ground
30	4AOUT14	A-BUS Bit 14
31	4AOUT15	A-BUS Bit 15
32	4AOUT16	A-BUS Bit 16
33	4AOUT17	A-BUS Bit 17
34	GND	Ground
35	4AOUT18	A-BUS Bit 18
36	4AOUT19	A-BUS Bit 19
37	4AOUT20	A-BUS Bit 20
38	4AOUT21	A-BUS Bit 21
39	GND	Ground
40	4AOUT22	A-BUS Bit 22

TABLE 2-3. (Continued) CONNECTOR LIST
MODEL 482M CONNECTOR J01
MEZZANINE

PIN	SIGNAL	FUNCTION
41	4AOUT23	A-BUS Bit 23
42	4AOUT24	A-BUS Bit 24
43	4AOUT25	A-BUS Bit 25
44	GND	Ground
45	4AOUT26	A-BUS Bit 26
46	4AOUT27	A-BUS Bit 27
47	4AOUT28	A-BUS Bit 28
48	4AOUT29	A-BUS Bit 29
49	GND	Ground
50	4AOUT30	A-BUS Bit 30
51	4AOUT31	A-BUS Bit 31
52	GND	Ground
53	GND	Ground
54	9AOSTRB	A-BUS Data Strobe
55	GND	Ground
56	GND	Ground
57	5AOACKM	A-BUS Acknowledge Mezzanine
58	5AOREQM	A-BUS Request Mezzanine
59	GND	Ground
60	GND	Ground
61	5MLBRST	Mezzanine Local Bus Reset
62	MLBWRT	Mezzanine Local Bus Write
63	5MEZZCS	Mezzanine Chip Select-
64	MLBAD2	Mezzanine Local Bus Address 2
65	MLBAD3	Mezzanine Local Bus Address 3
66	MLBAD4	Mezzanine Local Bus Address 4
67	MLBAD5	Mezzanine Local Bus Address 5
68	MLBAD6	Mezzanine Local Bus Address 6
69	MZTAK	Mezzanine Time Acknowledge
70	MLBD0	Mezzanine Local Bus Data 0
71	MLBD1	Mezzanine Local Bus Data 1
72	MLBD2	Mezzanine Local Bus Data 2
73	MLBD3	Mezzanine Local Bus Data 3
74	MLBD4	Mezzanine Local Bus Data 4
75	MLBD5	Mezzanine Local Bus Data 5
76	MLBD6	Mezzanine Local Bus Data 6
77	GND	Ground
78	MLBD7	Mezzanine Local Bus Data 7
79	MLBD8	Mezzanine Local Bus Data 8
80	MLBD9	Mezzanine Local Bus Data 9

TABLE 2-3. (Continued) CONNECTOR LIST
MODEL 482M CONNECTOR J01
MEZZANINE

PIN	SIGNAL	FUNCTION
81	MLBD10	Mezzanine Local Bus Data 10
82	MLBD11	Mezzanine Local Bus Data 11
83	MLBD12	Mezzanine Local Bus Data 12
84	MLBD13	Mezzanine Local Bus Data 13
85	MLBD14	Mezzanine Local Bus Data 14
86	MLBD15	Mezzanine Local Bus Data 15
87	5MEZDRY	Mezzanine Ready-
88	MZTRUN	Mezzanine Time Run
89	VCC5	+5Vdc
90	GND	Ground
91	VCC5	+5Vdc
92	GND	Ground
93	-VCC12	-12Vdc
94	GND	Ground
95	-VCC12	-12Vdc
96	GND	Ground
97	+VCC12	+12Vdc
98	GND	Ground
99	+VCC12	+12Vdc
100	GND	Ground

TABLE 2-4. CONNECTOR LIST
MODEL 482M FRONT PANEL CONNECTOR RC1
EXTERNAL DTOA AND LINES OUT

PIN	SIGNAL	FUNCTION
01	4DCOT00	DTOA OUT 00
02	4DCOT01	DTOA OUT 01
03	4DCOT02	DTOA OUT 02
04	4DCOT03	DTOA OUT 03
05	4DCOT04	DTOA OUT 04
06	4DCOT05	DTOA OUT 05
07	4DCOT06	DTOA OUT 06
08	4DCOT07	DTOA OUT 07
09	4DCOT08	DTOA OUT 08
10	4DCOT09	DTOA OUT 09
11	4DCOT10	DTOA OUT 10
12	4DCOT11	DTOA OUT 11
13	4DCOT12	DTOA OUT 12
14	4DCOT13	DTOA OUT 13
15	4DCOT14	DTOA OUT 14
16	4DCOT15	DTOA OUT 15
17	*LINE00	LINE OUT 00
18	*LINE01	LINE OUT 01
19	*LINE02	LINE OUT 02
20	*LINE03	LINE OUT 03
21	*LINE04	LINE OUT 04
22	*LINE05	LINE OUT 05
23	*LINE06	LINE OUT 06
24	*LINE07	LINE OUT 07
25	*LINE08	LINE OUT 08
26	*LINE09	LINE OUT 09
27	*LINE10	LINE OUT 10
28	*LINE11	LINE OUT 11
29	*LINE12	LINE OUT 12
30	*LINE13	LINE OUT 13
31	*LINE14	LINE OUT 14
32	*LINE15	LINE OUT 15
33	$DATRY1	Discrete Strobe 1
34	$DATAK1	Discrete Acknowledge 1
35	GND	Ground
36	GND	Ground
37	GND	Ground
38	GND	Ground
39	GND	Ground
40	GND	Ground

* Assert polarity (4/9) determined by U31-6
$ Assert polarity (4/9) determined by U31-4 & -5

TABLE 2-4. (Continued) CONNECTOR LIST
MODEL 482M CONNECTOR RC1
EXTERNAL DTOA AND LINES OUT

PIN	SIGNAL	FUNCTION
41	GND	Ground
42	GND	Ground
43	GND	Ground
44	GND	Ground
45	GND	Ground
46	GND	Ground
47	GND	Ground
48	GND	Ground
49	GND	Ground
50	GND	Ground
51	GND	Ground
52	GND	Ground
53	GND	Ground
54	GND	Ground
55	GND	Ground
56	GND	Ground
57	GND	Ground
58	GND	Ground
59	GND	Ground
60	GND	Ground
61	GND	Ground
62	GND	Ground
63	GND	Ground
64	GND	Ground
65	GND	Ground
66	GND	Ground
67	GND	Ground
68	GND	Ground

TABLE 2-5. CONNECTOR LIST
MODEL 482M CONNECTOR RC2
INTERNAL DTOA AND LINES OUT

PIN	SIGNAL	FUNCTION
01	GND	Ground
02	$DATAK2	Discrete Acknowledge 2
03	GND	Ground
04	$DATRY2	Discrete Strobe 2
05	GND	Ground
06	*LINE31	LINE OUT 31
07	GND	Ground
08	*LINE30	LINE OUT 30
09	GND	Ground
10	*LINE29	LINE OUT 29
11	GND	Ground
12	*LINE28	LINE OUT 28
13	GND	Ground
14	*LINE27	LINE OUT 27
15	GND	Ground
16	*LINE26	LINE OUT 26
17	GND	Ground
18	*LINE25	LINE OUT 25
19	GND	Ground
20	*LINE24	LINE OUT 24
21	GND	Ground
22	*LINE23	LINE OUT 23
23	GND	Ground
24	*LINE22	LINE OUT 22
25	GND	Ground
26	*LINE21	LINE OUT 21
27	GND	Ground
28	*LINE20	LINE OUT 20
29	GND	Ground
30	*LINE19	LINE OUT 19
31	GND	Ground
32	*LINE18	LINE OUT 18
33	GND	Ground
34	*LINE17	LINE OUT 17
35	GND	Ground
36	*LINE16	LINE OUT 16

* Assert polarity (4/9) determined by U31-6
$ Assert polarity (4/9) determined by U31-4 & -5

TABLE 2-5. (Continued) CONNECTOR LIST
MODEL 482M CONNECTOR RC2
INTERNAL DTOA AND LINES OUT

PIN	SIGNAL	FUNCTION
37	GND	Ground
38	4DCOT31	DTOA OUT 31
39	GND	Ground
40	4DCOT30	DTOA OUT 30
41	GND	Ground
42	4DCOT29	DTOA OUT 29
43	GND	Ground
44	4DCOT28	DTOA OUT 28
45	GND	Ground
46	4DCOT27	DTOA OUT 27
47	GND	Ground
48	4DCOT26	DTOA OUT 26
49	GND	Ground
50	4DCOT25	DTOA OUT 25
51	GND	Ground
52	4DCOT24	DTOA OUT 24
53	GND	Ground
54	4DCOT23	DTOA OUT 23
55	GND	Ground
56	4DCOT22	DTOA OUT 22
57	GND	Ground
58	4DCOT21	DTOA OUT 21
59	GND	Ground
60	4DCOT20	DTOA OUT 20
61	GND	Ground
62	4DCOT19	DTOA OUT 19
63	GND	Ground
64	4DCOT18	DTOA OUT 18
65	GND	Ground
66	4DCOT17	DTOA OUT 17
67	GND	Ground
68	4DCOT16	DTOA OUT 16

TABLE 2-6. CONNECTOR LIST
MODEL 482M CONNECTOR RC3
ANALOG 00-15 INPUT

PIN	SIGNAL	FUNCTION
01	GND	Ground
02	GND	Ground
03	4INPA00	Analog Input 00 +
04	9INPA00	Analog Input 00 -
05	GND	Ground
06	GND	Ground
07	4INPA02	Analog Input 02 +
08	9INPA02	Analog Input 02 -
09	GND	Ground
10	GND	Ground
11	4INPA04	Analog Input 04 +
12	9INPA04	Analog Input 04 -
13	GND	Ground
14	GND	Ground
15	4INPA06	Analog Input 06 +
16	9INPA06	Analog Input 06 -
17	GND	Ground
18	GND	Ground
19	4INPA08	Analog Input 08 +
20	9INPA08	Analog Input 08 -
21	GND	Ground
22	GND	Ground
23	4INPA10	Analog Input 10 +
24	9INPA10	Analog Input 10 -
25	GND	Ground
26	GND	Ground
27	4INPA12	Analog Input 12 +
28	9INPA12	Analog Input 12 -
29	GND	Ground
30	GND	Ground
31	4INPA14	Analog Input 14 +
32	9INPA14	Analog Input 14 -

TABLE 2-6. (Continued) CONNECTOR LIST
MODEL 482M CONNECTOR RC3
ANALOG 00-16 INPUT

PIN	SIGNAL	FUNCTION
33	GND	Ground
34	GND	Ground
35	4INPA01	Analog Input 01 +
36	9INPA01	Analog Input 01 -
37	GND	Ground
38	GND	Ground
39	4INPA03	Analog Input 03 +
40	9INPA03	Analog Input 03 -
41	GND	Ground
42	GND	Ground
43	4INPA05	Analog Input 05 +
44	9INPA05	Analog Input 05 -
45	GND	Ground
46	GND	Ground
47	4INPA07	Analog Input 07 +
48	9INPA07	Analog Input 07 -
49	GND	Ground
50	GND	Ground
51	4INPA09	Analog Input 09 +
52	9INPA09	Analog Input 09 -
53	GND	Ground
54	GND	Ground
55	4INPA11	Analog Input 11 +
56	9INPA11	Analog Input 11 -
57	GND	Ground
58	GND	Ground
59	4INPA13	Analog Input 13 +
60	9INPA13	Analog Input 13 -
61	GND	Ground
62	GND	Ground
63	4INPA15	Analog Input 15 +
64	9INPA15	Analog Input 15 -
65	GND	Ground
66	GND	Ground
67		
68		

TABLE 2-7. CONNECTOR LIST
MODEL 482M CONNECTOR TC1
TEST

PIN	SIGNAL	FUNCTION
01	GND	Ground
02	ACIPRB	
03	ACIPRA	
04	ACITCK	
05	ACITD1	
06	ACITMS	
07	TDOTC1	

TABLE 2-8. CONNECTOR LIST
MODEL 482M CONNECTOR U5
DAC BUS FIBER OPTIC OUTPUT

PIN	SIGNAL	FUNCTION
01		Fiber Optic Output
02	GND	Ground

TABLE 2-9. REAR PANEL SIGNAL LIST
CABLE FOR MODEL 482M-32 (PN 1716422-14)
Mates with 482M connector RC2
EXTERNAL DTOA & LINES OUT 16-31

PIN	SIGNAL	FUNCTION
01	4DCOT16	DTOA OUT 16
02	4DCOT17	DTOA OUT 17
03	4DCOT18	DTOA OUT 18
04	4DCOT19	DTOA OUT 19
05	4DCOT20	DTOA OUT 20
06	4DCOT21	DTOA OUT 21
07	4DCOT22	DTOA OUT 22
08	4DCOT23	DTOA OUT 23
09	4DCOT24	DTOA OUT 24
00	4DCOT25	DTOA OUT 25
11	4DCOT26	DTOA OUT 26
12	4DCOT27	DTOA OUT 27
13	4DCOT28	DTOA OUT 28
14	4DCOT29	DTOA OUT 29
15	4DCOT30	DTOA OUT 30
16	4DCOT31	DTOA OUT 31
17	*LINE16	LINE OUT 16
18	*LINE17	LINE OUT 17
19	*LINE18	LINE OUT 18
20	*LINE19	LINE OUT 19
21	*LINE20	LINE OUT 20
22	*LINE21	LINE OUT 21
23	*LINE22	LINE OUT 22
24	*LINE23	LINE OUT 23
25	*LINE24	LINE OUT 24
26	*LINE25	LINE OUT 25
27	*LINE26	LINE OUT 26
28	*LINE27	LINE OUT 27
29	*LINE28	LINE OUT 28
30	*LINE29	LINE OUT 29
31	*LINE30	LINE OUT 30
32	*LINE31	LINE OUT 31
33	$DATRY2	Discrete Strobe 2
34	$DATAK2	Discrete Acknowledge 2

* Assert polarity (4/9) determined by U31-6
$ Assert polarity (4/9) determined by U31-4 & -5

TABLE 2-9.(Continued) SIGNAL LIST
CABLE FOR MODEL 482M-32 (PN 1716422-14)
Mates with 482M connector RC2
EXTERNAL DTOA & LINES OUT 16-31

PIN	SIGNAL	FUNCTION
35	GND	Ground (D16)
36	GND	Ground (D17)
37	GND	Ground (D18)
38	GND	Ground (D19)
39	GND	Ground (D20)
40	GND	Ground (D21)
41	GND	Ground (D22)
42	GND	Ground (D23)
43	GND	Ground (D24)
44	GND	Ground (D25)
45	GND	Ground (D26)
46	GND	Ground (D27)
47	GND	Ground (D28)
48	GND	Ground (D29)
49	GND	Ground (D30)
50	GND	Ground (D31)
51	GND	Ground (L16)
52	GND	Ground (L17)
53	GND	Ground (L18)
54	GND	Ground (L19)
55	GND	Ground (L20)
56	GND	Ground (L21)
57	GND	Ground (L22)
58	GND	Ground (L23)
59	GND	Ground (L24)
60	GND	Ground (L25)
61	GND	Ground (L26)
62	GND	Ground (L27)
63	GND	Ground (L28)
64	GND	Ground (L29)
65	GND	Ground (L30)
66	GND	Ground (L31)
67	GND	Ground (STRB)
68	GND	Ground (ACK)

TABLE 2-10. REAR PANEL SIGNAL LIST
CABLE FOR MODELS 482M-32 (PN 1716422-18)
Mates with 482M connector RC3
ANALOG 00-15 INPUTS

PIN	SIGNAL	FUNCTION
68	GND	Ground
34	GND	Ground
67	4INPA00	Analog Input 00 +
33	9INPA00	Analog Input 00 -
66	GND	Ground
32	GND	Ground
65	4INPA02	Analog Input 02 +
31	9INPA02	Analog Input 02 -
64	GND	Ground
30	GND	Ground
63	4INPA04	Analog Input 04 +
29	9INPA04	Analog Input 04 -
62	GND	Ground
28	GND	Ground
61	4INPA06	Analog Input 06 +
27	9INPA06	Analog Input 06 -
60	GND	Ground
26	GND	Ground
59	4INPA08	Analog Input 08 +
25	9INPA08	Analog Input 08 -
58	GND	Ground
24	GND	Ground
57	4INPA10	Analog Input 10 +
23	9INPA10	Analog Input 10 -
56	GND	Ground
22	GND	Ground
55	4INPA12	Analog Input 12 +
21	9INPA12	Analog Input 12 -
54	GND	Ground
20	GND	Ground
53	4INPA14	Analog Input 14 +
19	9INPA14	Analog Input 14 -

TABLE 2-10. (Continued) SIGNAL LIST
CABLE FOR MODEL 482M-32 (PN 1716422-18)
Mates with 482M connector RC3
ANALOG 00-15 INPUTS

PIN	SIGNAL	FUNCTION
52	GND	Ground
18	GND	Ground
51	4INPA01	Analog Input 01 +
17	9INPA01	Analog Input 01 -
50	GND	Ground
16	GND	Ground
49	4INPA03	Analog Input 03 +
15	9INPA03	Analog Input 03 -
48	GND	Ground
14	GND	Ground
47	4INPA05	Analog Input 05 +
13	9INPA05	Analog Input 05 -
46	GND	Ground
12	GND	Ground
45	4INPA07	Analog Input 07 +
11	9INPA07	Analog Input 07 -
44	GND	Ground
10	GND	Ground
43	4INPA09	Analog Input 09 +
09	9INPA09	Analog Input 09 -
42	GND	Ground
08	GND	Ground
41	4INPA11	Analog Input 11 +
07	9INPA11	Analog Input 11 -
40	GND	Ground
06	GND	Ground
39	4INPA13	Analog Input 13 +
05	9INPA13	Analog Input 13 -
38	GND	Ground
04	GND	Ground
37	4INPA15	Analog Input 15 +
03	9INPA15	Analog Input 15 -
36	GND	Ground
02	GND	Ground
35		
01		

SECTION 3
OPERATION

3.1 INTRODUCTION

The host processor interfaces the Model 482M DAC/ADC card through twenty 32-bit registers that are offset 0x100 from the PDSP Setup & Control registers - which are in turn mapped into the PCI address space relative to PCI *System Configuration Base Address Registers* 2 or 3. Setup information is only in the 16 least significant bits of the 32-bit word.

3.2 SETUP REGISTERS

The setup registers are listed in TABLE 3-1, and are briefly described in the following paragraphs

3.2.1 Signature Register (Address 100)

The first register is the Signature Register, and is located at byte address 0x100. When read, the register returns 0X *0482* or *1482*. Switch 7 of U31 defines the available options. Setting switch 7 to OFF will return a signature of 0482, while setting it to ON returns 1482. The first hex digit identifies the card option, with zero indicating the 482M-32 card containing 32 analog outputs, 32 discrete lines, 16 analog inputs. A one indicates the 482M-8 card, containing eight analog outputs and eight discrete lines. The hex *482* indicates that a mezzanine card is installed.

3.2.2 DAC Page Address Reg. & Switch Override (Address 104)

Bits 0-6 form the *page offset* that selects any one of the 128 pages (32 DAC and 32 discrete channels per page) you can address over the A-bus. The page register is initialized to page zero. You can also control the external switch settings (provided by U31 positions 1-8, see section 5.1.1.1) with bits 7-15. Bit 7 set to **0** will allow switch U31 positions 1-8 to control discrete line options and select Test Mode.

Bit 7 set to **1** overrides all switch settings and replaces them with a configurable setting specified by bits 8-15, which correspond to SW1 thru SW8 on U31, as shown below.

Register bits 8 & 9 control timing per the following table.

DISCRETE LINE TRANSFER CONTROL MODE			
Bit 8	**Bit 9**	**MODE**	**DESCRIPTION**
OFF	OFF	0	NO Control Strobe (*DATRY1 or 2)
OFF	ON	1	*DATRY1 or 2 is set for 125 or 250ns
ON	OFF	2	*DATAK1 or 2 enables *DATRY1 or 2
ON	ON	3	Full handshake

* Data Ready polairty is determined by bit 11, and Acknowledge polarity by bit 12.

Bit 10 selects the clock rate to the sequencer as follows;

DISCRETE LINE SEQUENCER CLOCK SELECTION	
Bit 10	**DESCRIPTION**
ON	the minimum setup & Data Strobe duration set to 125ns
OFF	the minimum setup & Data Strobe duration set to 250ns

Bits 11 & 12 select the polarity of discrete line control data ready signals as follows.

DISCRETE LINE CONTROL SIGNAL ASSERTION POLARITY		
Bit 11	**Bit 12**	**DESCRIPTION**
ON	X	HIGH Control Strobe for Discrete Lines 4DATRY1 or 2
OFF	X	LOW Control Strobe for Discrete Lines 9DATRY1 or 2
X	ON	HIGH assert level for Acknowledge Lines 4DATAK1 or 2
X	OFF	LOW assert level for Acknowledge Lines 9DATAK1 or 2

Bit 13 selects the discrete output polarity as follows;

DISCRETE LINE OUTPUT POLARITY	
Bit 8	**DESCRIPTION**
ON	Inverts the polarity of the discrete lines (the discrete lines become 9LINE00-31)
OFF	Selects high-asserted discrete lines (the discrete lines become 4LINE00-31)

U31 Switch 7 contains the card configuration and is always read in bit 12 of the Signature Register, therefore bit 14 in the Configuration Register is not used. You read the option selection in bit 12 of the Signature Register.

Bit 15 selects the test mode. When set to **1** bits 8 and 9 select one of three test modes as shown below.

MODE TEST SELECT			
Bit 15	**Bit14**	**Bit13**	**MODE**
ON	OFF	OFF	0
ON	OFF	ON	1
ON	ON	OFF	2

MODE 0: A 60 Hz ramp wave is sent to all DAC and Discrete channels.

MODE 1: A five step calibrate function steps from zero scale to full scale at one second intervals, sent to all DAC and discrete channels simultaneously.

MODE 2: All 16 A to D channels are scanned at 50kHz and output to the corresponding DAC channel. Since there are 16 A to D channels to 32 DAC channels, A to D channel 0 is sent to DAC0 & DAC16, A to D channel 1 is sent to DAC1 & DAC17, etc.

3.2.3 A to D Converter ID Offset (Address 108)

Bits 0 to 12 of this register supply the 13 most significant bits of the 17-bit ID tag. The four least significant bits are provided by the A to D channel address. The register defaults to 0X01FC.

MODEL 482M DAC/ADC SETUP & CONTROL REGISTERS						
ADDR	**DESCRIPTION**	**15 14 13 12**	**11 10 9 8**	**7 6 5 4**	**3 2 1 0**	**MODE**
100	Signature	X	4	8	2	Read
102	Not used					
104	DAC Page Config	configuration |. page .				R/W
106	Not used					
108	A to D ID Offset	|. 13 MSBs of 17 bit ID tag .				R/W
10A	Not used					
10C	Not used					
10E	Not used					
110	CH 0 Rate Control	Channel 0 Control				R/W
112	Not used					
114	CH 1 Rate Control	Channel 1 Control				R/W
116	Not used					
118	CH 2 Rate Control	Channel 2 Control				R/W
11A	Not used					
11C	CH 3 Rate Control	Channel 3 Control				R/W
11E	Not used					
120	CH 4 Rate Control	Channel 4 Control				R/W
122	Not used					
124	CH 5 Rate Control	Channel 5 Control				R/W
126	Not used					
128	CH 6 Rate Control	Channel 6 Control				R/W
12A	Not used					
12C	CH 7 Rate Control	Channel 7 Control				R/W
12E	Not used					
130	CH 8 Rate Control	Channel 8 Control				R/W
132	Not used					
134	CH 9 Rate Control	Channel 9 Control				R/W
136	Not used					
138	CH 10 Rate Control	Channel 10 Control				R/W
13A	Not used					
13C	CH 11 Rate Control	Channel 11 Control				R/W
13E	Not used					
140	CH 12 Rate Control	Channel 12 Control				R/W
142	Not used					
144	CH 13 Rate Control	Channel 13 Control				R/W
146	Not used					
148	CH 14 Rate Control	Channel 14 Control				R/W
14A	Not used					
14C	CH 15 Rate Control	Channel 15 Control				R/W
14E	Not used					

TABLE 3-1. Model 482M DAC/ADC - Setup & Control Registers

3.2.4 A to D Sampling Rate Registers (Addresses 110 to 14C)

The Analog-to-Digital Converter option consists of additional circuitry installed on the 482M mezzanine card. The LSB of the high nibble of the card Signature Register indicates the presence of the A to D option by changing the signature from $1482_{hex.}$ to $0482_{hex.}$

The analog option provides sixteen differential inputs. Each input has a differential-to-single-ended amplifier. The inputs are multiplexed in sets of eight channels into two separate 12 bit A to D converters, each converter having a maximum composite conversion rate of 400,000 samples per second. Two Analog Devices 7891 converters perform the Analog to Digital conversion. One converter digitizes the odd channels, and the other does the even. This allows simultaneous sampling of paired channels (when equal sampling rates are selected), up to a maximum sampling rate of 400k samples per channel. There is a mode that allows you to connect one input signal to two paired channels, sampled at twice the selected sampling rate. This is done by skewing the sampling of the second channel by one half of the sampling interval, thus a sampling rate of 400k samples with offset sampling provides a single channel converted at 800k samples per second. The format of the sample control register for channel zero is shown in TABLE 3-2 following.

A TO D SAMPLING RATE CONTROL REGISTER															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	Format		R	Prescale			S	Rate Divider						
R = Reserved S = Skewed sample															

TABLE 3-2. A to D Sampling Rate Control Register

Programmable sampling intervals from 16 to 400,000 samples per second are available for each input. The channel rate is set by writing a 16 bit word of the following format: bits 0-6 contain a divider (from 1 to 128) that is set by entering a number between 0 and 127. Bit 7 is set to **1** to specify offset sampling, and bits 8-10 contain a prescalar whose values are shown in the table below.

RATE SETUP WORD PRESCALE - BITS 8, 9, 10 DECODE

Value	Clock Rate
7	16 MHz
6	4 MHz
5	1 MHz
4	250 kHz
3	50 kHz
2	10 kHz
1	2 kHz
0	Channel Disable

Bits 8, 9, and 10 of all channels default to zero at reset, disabling the channels.

Bits 12 & 13 at address 0X110 (Channel 0 Rate Control register) are reserved to select the data format. The values of bits 12 & 13 and the resulting output format are shown below. The data format defaults to zero at reset.

DATA FORMAT - BITS 12, 13 DECODE

Value	Description
3	Twos complement, Right justified
2	Twos complement, Left justified
1	Offset binary, Right justified
0	Offset binary, Left justified

Bits 11, 14, & 15 are reserved.

3.2.5 Programming Analog Sampling

The setup language for the analog channels is compatible with that used in the Acroamatics 2110 series Telemetry Data Processors. The following section discusses the setup syntax.

Standard TDP syntax is used to specify the data processing. The ID field (in this case, the ID is the channel number) must include a specification of the analog sampling rate. The schematic representation is

```
ANA
ID(rate):
                ⋮

END
```

rate is the sampling rate expressed in samples per second, and should lie between 16 and 400,000. The sum of all the sampling rates per channel should not exceed 400,000. If you exceed this rate, the data is sampled as rapidly as possible, with the total number of channels sampled at about 400,000 samples per second. This adjustment is made by the hardware by reducing the sampling rate on the higher speed channels as necessary. A rate of zero disables the channel.

The ID values for the analog channels are assigned using the programmed channel numbers relative to the base of 1FC0 hex (8128); therefore, channel 0 has output ID 8128, channel 1, output ID 8129, and channel 15, output ID 8143. You may list more than one ID on a line if the processing of the data is the same.

An example of Analog Port programming is

```
ANA
OBN       |data format is offset binary
2(10000):                FL1 2%
1(2000):  3:     PAS
4(5000): 5: 6: 7:        FL1 1%
END
```

Note the unexpressed sampling rate for channels 5, 6, and 7, which are sampled at the same rate (5000) as channel 4.

You can program the analog sampling rates and the data format with the command

RATE *[format] rate ...*

is the sampling rate in samples per second, 16 to 400000. A rate of zero disables the channel. A list of channels ... follows the rate, and all specified channels (0-15) are set to the specified rate. To use the RATE command to set the Data Format, use the options listed below. You set one format for all of the channels. If the format is not specified in the RATE command, it is not changed from its previous setting. At power up and reset, the format is offset binary, left justified.

Format Specifier	Data Format
RJA	Twos complement, Right justified
LJA	Twos complement, Left justified
RJL	Offset binary, Right justified
LJL	Offset binary, Left justified

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

FIGURE 4-1 is a simplified block diagram of all the functions available on the various 482M DAC/ADC mezzanine cards. The card provides 16 analog inputs, 32 analog outputs, 32 discrete lines (a fiber-optic DAC bus regenerator is not yet available). Dash numbered versions provide various combinations of the above. The following paragraphs contain a brief discription of the card functions.

4.2 ANALOG OPTION

The analog option provides sixteen differential inputs. Each input consists of a differential-to-single-ended amplifier. The amplifier outputs are multiplexed in sets of eight channels into two separate 12 bit A to D converters, each converter having a maximum composite conversion rate of 400,000 samples per second. Programmable sampling intervals from 16 to 400k samples per second are available for each input. Two Analog Devices 7891 converters perform Analog to Digital conversion, with one converter digitizing the odd channels, while the other does the even channels. This division allows simultaneous sampling of paired channels (when equal sampling rates are selected), up to a maximum sampling rate of 400k samples per channel. A mode is provided which allows you, by connecting one input signal to two paired channels, to sample that input signal at twice the selected sampling rate. This is done by skewing the sampling of the second channel by one half of the sampling interval, thus a sampling rate of 400k samples with offset (skewed) sampling provides a single channel converted at 800k samples per second. The digitized samples are assigned an ID tag that consists of the channel number and an offset value that you select in the A to D ID Offset Register (Address 0X108). This register defaults to 01FC at power on. The messages are output on the A-bus and addressed to the Feedback Port.

4.3 DAC BUS REGENERATOR

The 482M card optionally contains a fiber-optic, high speed serial, external extension of the DAC bus, which transfers over six million DAC messages per second over distances of over 1000 meters. All messages to Device 7 are captured as 32-bit messages, which are divided into four bytes and serialized by a CYPRESS CY7B923 HOTLink™ transmitter at 250 Mbits per second. The serial data stream is connected to an Aligent™ HFBR-1119T multimode fiber optic transmitter. External connections are made with a multimode fiber optic cable terminated with an ST connector.

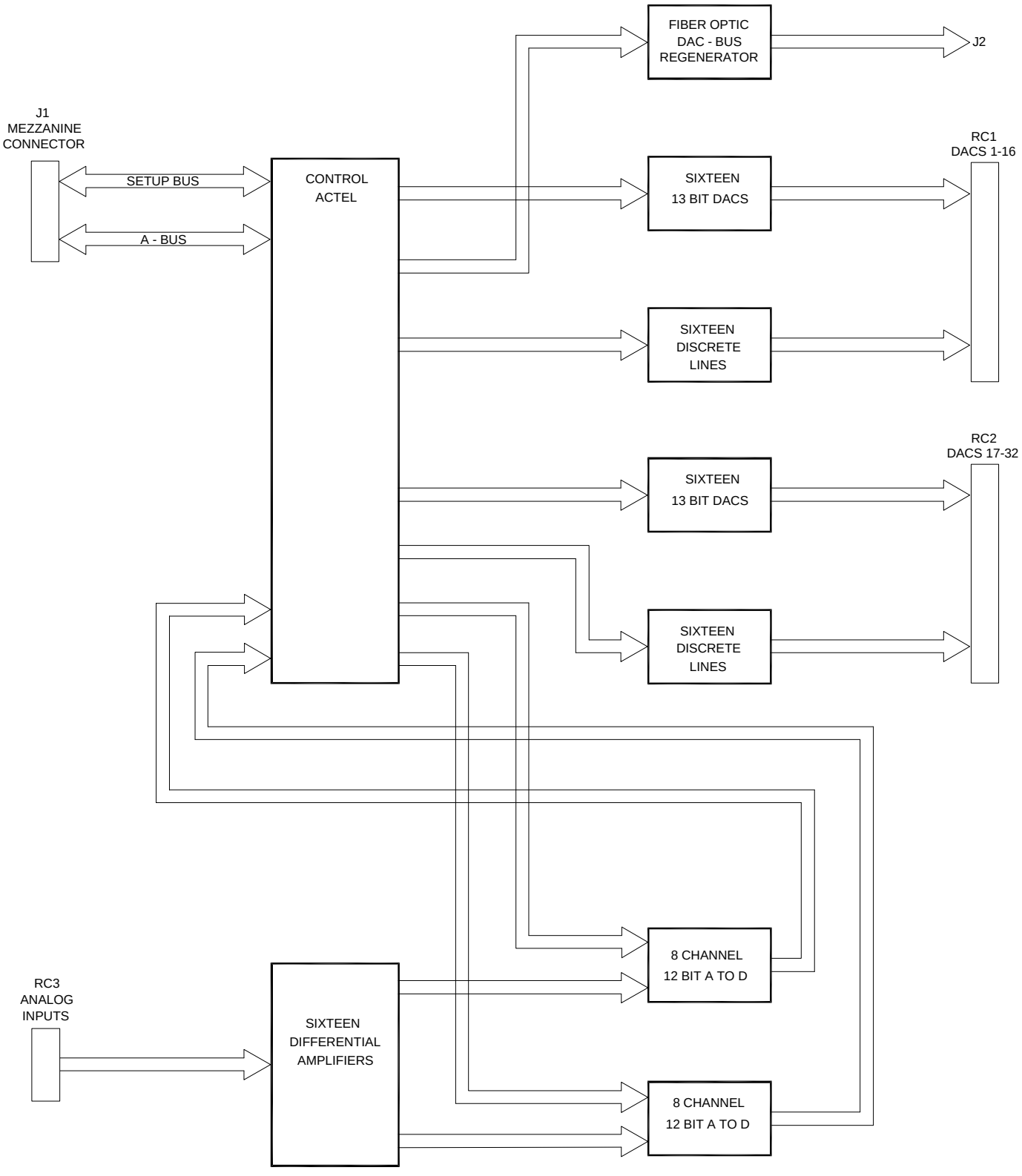


FIGURE 4-1 482 MEZZANINE SIMPLIFIED BLOCK DIAGRAM

4.4 ANALOG & DISCRETE LINE OUTPUTS

The 482M-8 version of the card contains eight analog outputs and eight discrete lines, while the 482M-32 version provides 32 analog outputs and 32 discrete lines. The first 16 (or all 8 on the 482M-8) analog channels are available at front panel connector RC1, and the second 16 are available at card edge connector RC2. The 32 analog outputs provide +5 to -5 Volt outputs. The 32 discrete lines each source up to 32ma and sink up to 64ma.

4.4.1 Messages to the DACs and Discrete Lines

32-bit messages are read from the A-bus when they are addressed to Device 7. The most significant word contains a 12-bit address on lines/bits 16 to 27 and control lines on bits 28 to 31; The least significant 16 bits contain the data message. The message format is shown in TABLES 4-1 to 4-3. A 12-bit address allows 4096 DACs and 4096 discrete lines to be addressed. Since there are only 32 DACs and 32 discretes on a 482M-32 card, the channel address is provided by the five LSBs (lines 16 to 20) and the seven MSBs (lines 21 to 27) are decoded to provide 128 possible card addresses. Card address selection is specified by bits 0 to 6 of the DAC Page Address Register (Address 0X104) when bits 0 to 6 match bits 20 to 27 of the DAC Select message.

The decode logic acts as a *card select* signal. This allows the DAC bus to address 128 cards, each providing 32 DACs and 32 discretes. Card selection is specified by bits 0 to 6 in the DAC Page Address Register. Bit 28 is set to **1** to indicate a discrete lines message. Bits 29 & 30 are encoded to perform a control function as shown in TABLE 4-2. When the message is discrete lines, the field selects 1-, 8-, or 16-bit discrete messages. When the message is to DAC channels the contents of this field inverts the data, sign, both, or specifies no inversion. Bit 31 provides a calibrate function. When bit 31 is set to **1**, the message is sent to all DACs and discrete lines regardless of the address field.

ADDRESS & MODE SELECT WORD FORMAT				
A-Bus I/O Buffer Register				
31	30 29	28	27	16
C	Mode	D	. 12 address lines	.

TABLE 4-1. Address & Mode Select Word Format for A-bus Messages to Device 7

MODE SELECTION		
30 - 29	**Discrete Line**	**DAC Output**
1 1	Not used	Invert Sign & Data
1 0	16 Bit	Invert Sign
0 1	8 Bit	Invert Data
0 0	1 Bit	No inversion

TABLE 4-2. Mode Selection

The 32-bit messages contain 16 bits of data in the least significant word. The data message is different for DAC channels and discrete channels, as shown in TABLE 4-3. A data message to the DACs is a left-justified, 13-bit, two's complement value with the sign in bit 15, and bits 0 to 2 are not used. When the data is a part of a discrete message, the format is determined by the discrete size, as defined in the control portion of the message. 16-bit discrete messages use bits 0 to 15. You can address a 16-bit discrete message to *discrete 0,* which will drive discrete lines 0 to 15, or to *discrete 16,* which will drive discrete lines 16 to 31.

You can address 8-bit discrete messages to *discrete 0, 8, 16,* or *24.* The data field is left-justified in bits 8 to 15. Messages to *Discrete 0* will drive discrete lines 0 to 7; to *Discrete 8* will drive discrete lines 8 to 15; to *Discrete 16* will drive lines 16 to 23, and to *Discrete 24,* lines 24 to 31. A one bit discrete is also left-justified in the data field, therefore expressed by the value of bit 15. The one bits have unique addresses from 0 to 31.

DATA WORD FORMAT															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC Data Location															
15 .					13 Bit DAC Data						.	3	2-unused-0		
Discrete 1 Bit Location															
D	14 .					not used								.	0
Discrete 8 Bit Location															
15 .			8 Bit Data			.	8	7 .			not used			.	0
Discrete 16 Bit Location															
15 .						16 Bit Data								.	0

TABLE 4-3. Data Word Format

4.4.2 Discrete Line Transfer Control & Timing

When you select the discrete lines for *16 bits per transfer,* you can use the Strobe (*DATRY1 or 2) and Acknowledge (*DATAK1 or 2) signals to synchronize discrete data transfers to an external device. You can use these control signals in any one of four modes, as determined by the setting of switch positions 1 and 2 of selector switch U31. Switch position 3 controls the interface timing signals and positions 4 & 5 control the polarities of the control signals. Switch 6 controls the polarity of the 32 discrete data lines.

4.4.2.1 Discrete Line Control Signals

When you use the discrete lines as 16 bit messages, you can use a control sequencer to both generate Data Ready strobes DATRDY1 or 2 and respond to Data Acknowledge signals DATACK1 or 2, thereby controlling message transfers to the external device. The sequencer-produced control signals are conditioned by Switches 1 and 2, and have durations determined by Switch 3.

The sequencer operates in four modes, controlled by switches 1 & 2 as shown in TABLE 4-4.

DISCRETE LINE TRANSFER CONTROL MODES			
SW2	**SW1**	**MODE**	**DESCRIPTION**
OFF	OFF	0	NO Control Strobe (*DATRY1 or 2)
OFF	ON	1	*DATRY1 or 2 is set for 125 or 250ns
ON	OFF	2	*DATAK1 or 2 enables *DATRY1 or 2
ON	ON	3	Full handshake
* 4 or 9 as selected by switches U31-3 & 4			

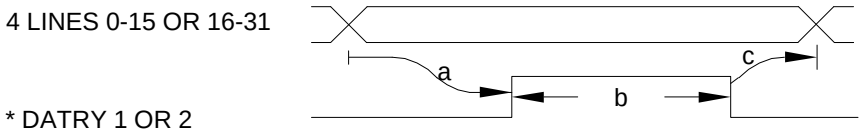
TABLE 4-4. Discrete Lines Transfer Control Modes

In MODE 1 the *Data Ready* control strobe is generated 125 or 250 nanoseconds after a change in the discrete data word, and remains set for 125 or 250 ns depending on the setting of U31-3.

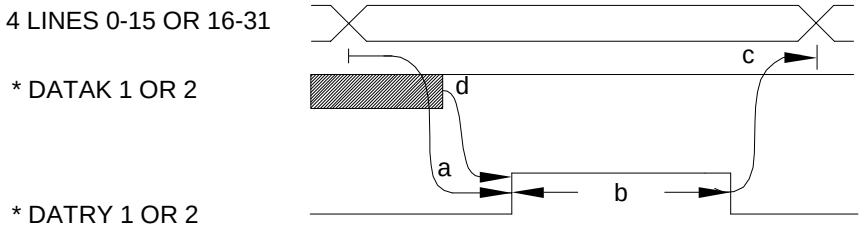
In MODE 2 the acknowledge signal *DATAK1 or 2 becomes a *READY* signal which must be asserted to enable the Data Output strobes *DATRY1 or 2.

In MODE 3 the *DATAK1 or 2 signals must be asserted to *enable* the *DATRY1 or 2 signals, and then de-asserted when DATRY1 or 2 is asserted to fully interlock the data transfer.

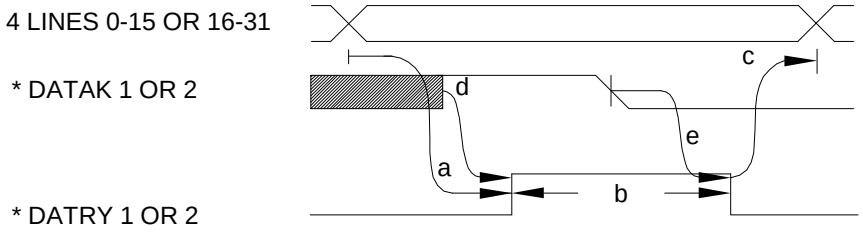
The timing requirements for Modes 1 - 3 are shown in FIGURE 4-2 on the following page.



MODE 1: DATA STROBE (*DATRY 1 OR 2) IS ENABLED BY A CHANGE IN LINES AND REMAINS ASSERTED FOR 125 OR 250 NANOSECONDS. THE DATA LINES REMAIN STABLE FOR A MINIMUM OF 62 NANOSECONDS AFTER THE TRAILING EDGE OF DATRY.



MODE 2: DATA STROBE (*DATRY 1 OR 2) IS ENABLED BY A CHANGE IN LINES AND ACKNOWLEDGE (*DATAK 1 OR 2) AND REMAINS ASSERTED FOR 125 OR 250 NANOSECONDS. THE DATA LINES REMAIN STABLE FOR A MINIMUM OF 62 NANOSECONDS AFTER THE TRAILING EDGE OF DATRY.



MODE 3: DATA STROBE (*DATRY 1 OR 2) IS ENABLED BY A CHANGE IN LINES AND ACKNOWLEDGE (*DATAK 1 OR 2) BEING ASSERTED DATA STROBE REMAINS ASSERTED FOR A MINIMUM OF 125 OR 250 NANOSECONDS AND REQUIRES THAT ACKNOWLEDGE IS DE-ASSERTED FOR A MINIMUM OF 62 NANOSECONDS PRIOR TO DE-ASSERTING DATA STROBE. THE DATA LINES REMAIN STABLE FOR A MINIMUM OF 62 NANOSECONDS AFTER THE TRAILING EDGE OF DATRY.

a = (125 NANOSECONDS Xn)
b = (125 NANOSECONDS Xn)
c = 62 NANOSECONDS MINIMUM
d = 62 NANOSECONDS MINIMUM
e = 62 NANOSECONDS MINIMUM
n = CLOCK SPEED 125 NANOSECONDS FOR SWITCH 3 ON.
250 NANOSECONDS FOR SWITCH 3 OFF.

* INDICATES THAT THE ASSERTED POLARITY IS CONTROLLED BY SWITCHES 4 & 5

FIGURE 4-2 DESCRETE LINE TIMING REQUIREMENTS DIAGRAM 7000224 REV. A

4.4.2.2 Discrete Control Signal Timing

Switch 3 determines signal timing by selecting the clock rate sent to the sequencer controlling discrete message transfers.

When Switch 3 is ON the minimum setup time from changing the data lines to the assertion of the output strobe is 125 ns and the minimum strobe duration is 125 ns.

When Switch 3 is OFF the above times are increased to 250 ns.

4.4.2.3 Data Ready Control Signal Assertion Polarity Switch 4

Switch 4 set ON selects HIGH assertion levels for the control strobe signals for discrete lines 0-31, and produces the signals 4DATRY1 & 4DATRY2.

Switch 4 set OFF selects LOW assertion levels for the discrete lines 0-31 Control strobe, and also produces the signals 9DATRY1 & 9DATRY2.

4.4.2.4 Acknowledge Signal Assertion Polarity Switch 5

Switch 5 set ON selects HIGH assertion levels for the discrete lines 0-31 Acknowledge strobe, and also produces the signals 4DATAK1 & 4DATAK2.

Switch 5 set OFF selects LOW assertion levels for the discrete lines 0-31 Acknowledge strobe, and also produces the signals 9DATAK1 & 9DATAK2.

4.4.2.5 Discrete Data Polarity Switch 6

Switch 6 set ON inverts the output data to the discrete lines, and set OFF non-inverts the output data to the discrete lines.

4.5 TEST MODES

Setting U31 switch eight to the ON position selects a test feature that overrides the normal functions of switch 1 and 2 (Discrete line handshake controls) to provide three separate test modes, as below.

MODE TEST SELECT			
Bit 15	**Bit14**	**Bit13**	**MODE**
ON	OFF	OFF	0
ON	OFF	ON	1
ON	ON	OFF	2

MODE 0: A 60 Hz ramp wave is sent to all DAC and Discrete channels.

MODE 1: A five step calibrate function steps from zero scale to full scale at one second intervals, sent to all DAC and discrete channels simultaneously.

MODE 2: All 16 A to D channels are scanned at 50kHz and output to the corresponding DAC channel. Since there are 16 A to D channels to 32 DAC channels, A to D channel 0 is sent to DAC0 & DAC16, A to D channel 1 is sent to DAC1 & DAC17, etc.

SECTION 5
ADJUSTABLE SWITCH SETTINGS

5.1 DESCRIPTION

The paragraphs below describe the selections available on the 482M Mezzanine DAC/ADC card.

5.1.1 Adjustable Switch Settings & Reference Voltage Adjustment

The 482M card contains an eight position selector switch at U31. Switches 1 - 6 select options for the discrete lines, Switch 7 reflects the available card configurations, and Switch 8 is for factory adjustment, described in Chapter 4.

FIGURE 5-1 shows the location of U31.

5.1.1.1 Switch U31

U31 Switches 1 & 2 control timing per the following;

U31 - DISCRETE LINE TRANSFER CONTROL MODE			
SW1	**SW2**	**MODE**	**DESCRIPTION**
OFF	OFF	0	NO Data Strobe (*DATRY1 or 2)
OFF	ON	1	*DATRY1 or 2 is set for 125 or 250ns
ON	OFF	2	*DATAK1 or 2 enables *DATRY1 or 2
ON	ON	3	Full handshake

* Data Ready polarity is determined by switch 4, Acknowledge polarity by switch 5. U31 Switch 3 selects the clock rate to the sequencer as follows;

U31 - DISCRETE LINE SEQUENCER CLOCK SELECTION	
SW3	**DESCRIPTION**
ON	the minimum setup & Data Strobe duration set to 125ns
OFF	the minimum setup & Data Strobe duration set to 250ns

U31 Switches 4 & 5 set the polarity of discrete line control Data Ready signals as follows;

U31 - CONTROL SIGNAL ASSERTION POLARITY		
SW4	**SW5**	**DESCRIPTION**
ON	X	HIGH Data Ready Strobe for Discrete Lines 4DATRY1 or 2
OFF	X	LOW Data Ready Strobe for Discrete Lines 9DATRY1 or 2
X	ON	HIGH assert level for Acknowledge Lines 4DATAK1 or 2
X	OFF	LOW assert level for Acknowledge Lines 9DATA1 or 2

U31 Switch 6 sets the discrete output polarity as follows;

U31 - DISCRETE LINE OUTPUT POLARITY	
SW6	**DESCRIPTION**
ON	Inverts the polarity of the discrete lines (the discrete lines become 9LINE00-31)
OFF	Selects high-asserted discrete lines (the discrete lines become 4LINE00-31)

U31 Switch 7 indicates the card configuration as follows;

U31 - 482M CARD CONFIGURATION	
SW7	**DESCRIPTION**
OFF	Card provides 32 analog outputs, 32 discrete lines, 16 analog inputs, and the external DAC Bus
ON	Card provides eight analog outputs & eight discrete lines only

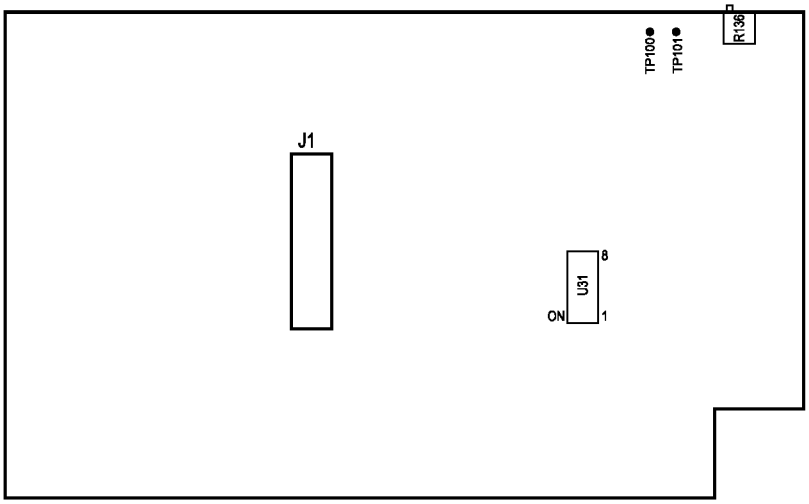
U31 Switch 8 is for test, and is described in Chapter 4.

5.2 REFERENCE VOLTAGE ADJUSTMENT

Connect a Voltmeter between TP100 (plus lead) and TP101. TP locations are shown in FIGURE 5-2. Adjust trimpot R136 for 5 Volts ± 1 millivolt.

5.2.1 Factory Settings

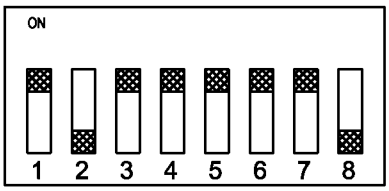
FIGURE 5-1 contains a record of the factory settings when your board was shipped.



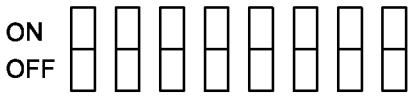
COMPONENT SIDE

ON = 0

OFF = 1



U31



SHIPPED AS _____

CARD 6011482 _____

SERIAL# / REV. _____

_____

CUSTOMER JOB#

_____

CONFIGURED BY DATE

_____

QC CHECK BY DATE

SELECTOR SWITCH U31 FUNCTIONS		
SWITCH U31	DESCRETE LINE TRANSFER CONTROL MODES	
1=OFF 2=OFF	MODE 0	NO CONTROL STROBE (*DATRY 1 OR 2)
1=ON 2=OFF	MODE 1	*DATRI 1 OR 2 SET FOR 125 OR 250 nS
1=OFF 2=ON	MODE 2	*DATAK 1 OR 2 ENABLE *DATRY 1 OR 2
1=ON 2=ON	MODE 3	FULL HANDSHAKE
SWITCH U31	DESCRIPTION	
3 ON	THE MINIMUM TIME FROM DISCRETE LINE CHANGE TO DATA READY IS 125 nS	
3 OFF	THE MINIMUM TIME FROM DISCRETE LINE CHANGE TO DATA READY IS 250 nS	
4 ON	SELECTS HIGH ASSERTION LEVELS FOR DATA READY SIGNALS (4DATRY 1 & 2)	
4 OFF	SELECTS LOW ASSERTION LEVELS FOR DATA READY SIGNALS (9DATRY 1 & 2)	
5 ON	SELECTS HIGH ASSERTION LEVELS FOR DATA ACKNOWLEDGE SIGNALS (4DATAK 1 & 2)	
5 OFF	SELECTS LOW ASSERTION LEVELS FOR DATA ACKNOWLEDGE SIGNALS (9DATAK 1 & 2)	
6 ON	INVERTS THE DISCRETE LINE OUTPUTS (9LINE00-31)	
6 OFF	NORMAL DISCRETE LINE OUTPUTS (4LINE00-31)	
7 ON	CARD HAS 8 DAC AND 16 DISCRETE LINES	
7 OFF	CARD HAS 32 DAC, 32 DISCRETES, 16 A TO D AND DAC BUS OUTPOUT	
8 ON	TEST MODE (SEE SECTION 4 FOR DESCRIPTION)	
8 OFF	NORMAL OPERATION	

*ASSERTION LEVEL (4 OR 9) SELECTED BY SWITCHES 4 AND 5

FIGURE 5-1. MEZZANINE DTOA OPTION SELECTOR SWITCHES

SECTION 6
DRAWINGS

6.1 INTRODUCTION TO THE 6011482-12 DRAWINGS

Section 6 contains a complete technical drawing package describing your 482M Mezzanine card. the drawings in this section are keyed to your specific serial numbered card.

6.1.1 Drawing System

Acroamatics Drawing numbers are seven digit numbers which can also have a two digit dash number. The first four digits represent a drawing class, and wherever a drawing may be part of a standard drawing package, drawing numbers are issued so that all drawings which are part of the package share the same last three digits. In the following discussion "xxx" represents the number keyed to the the card part number (6011xxx). Individual parts are classified within the same drawing system, but are assigned serially without regard to other assemblies.

The PC Card Reference package includes the following drawings:

FOR CARD PART NUMBER 60115xx:

60115xx	Card Assembly Drawing
81115xx	Card List of Materials
21115xx	Card Schematic Drawing

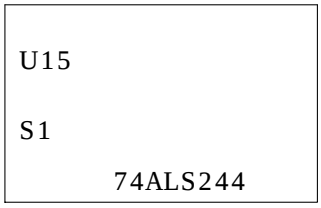
6.1.2 Drawing Package Organization

This section of the manual contains the physical drawings, called **Drawings**, as opposed to the schematic drawings, called **Schematics**, which are found in Section 7.

The Drawings section includes the card component assembly drawing 60115nn and the card List Of Materials (LOM). LOM's include sufficient information to facilitate ordering replacement parts either from Acroamatics or from the original component manufacturer. LOMs list parts by Acroamatics Part Number in the column headed **PART NO .** The component manufacturer is identified as **VENDOR**. Parts for which ACROAMATICS is listed as vendor are proprietary components available only from Acroamatics, Inc. Integrated Circuits which are industry standard are listed as GENERIC, and may be obtained from any reliable vendor. Other parts for which a specific source is listed may be available from other sources. When substituting parts from vendors other than those specifically listed, be certain that the components are truly interchangeable.

The last column (Reference) of the List of Materials lists the assembly location or locations. An assembly location can contain a socket as well as the component plugged into the socket.

For example

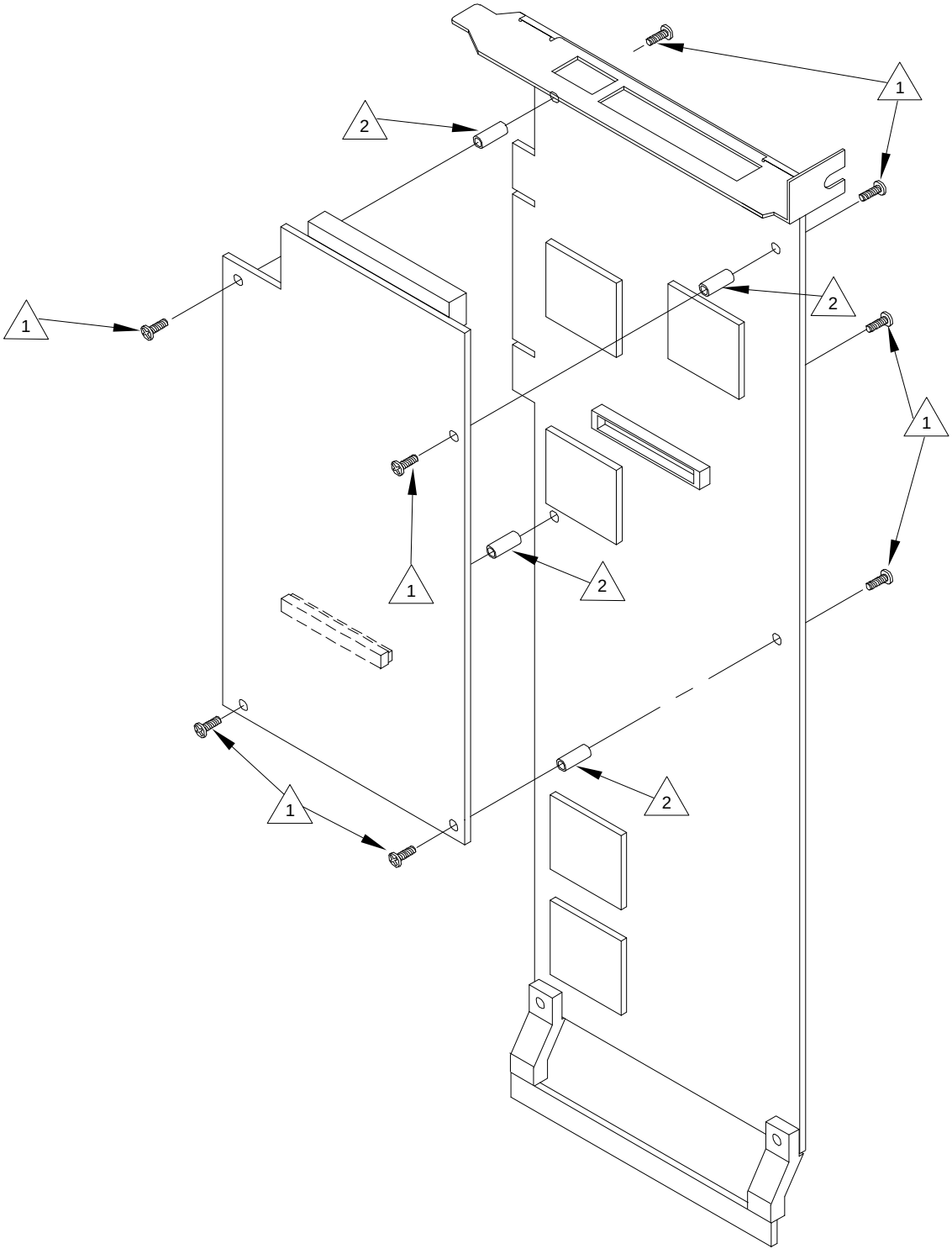


This example shows that location U15 contains socket S1 and an IC of type 74ALS244. Resistors, capacitors, and other components are shown in a similar fashion, and are referenced using common industry abbreviations.

6.1.3 Programmed Parts

The VME card can include programmed parts such as PROMs, EPROMs, EEPROMs, PALs, GALs, FPGAs, etc. If these are a permanent part of the hardware, they are documented on the List Of Materials for the PC card on which they are installed. Programmed parts are listed on the LOM twice; once as the unprogrammed part, with the Manufacturers Part Number, and also under the Acroamatics program number (606xxxx) with which they must be programmed to become the correct programmed part.

Programs for PROMs have part numbers in the series 6061xxx
Programs for EPROMs and EEPROMs have part numbers in the series 6062xxx
Programs for PALws and GALs have part numbers in the series 6064xxx
Programs for FPGAs have part numbers in the series 6067xxx



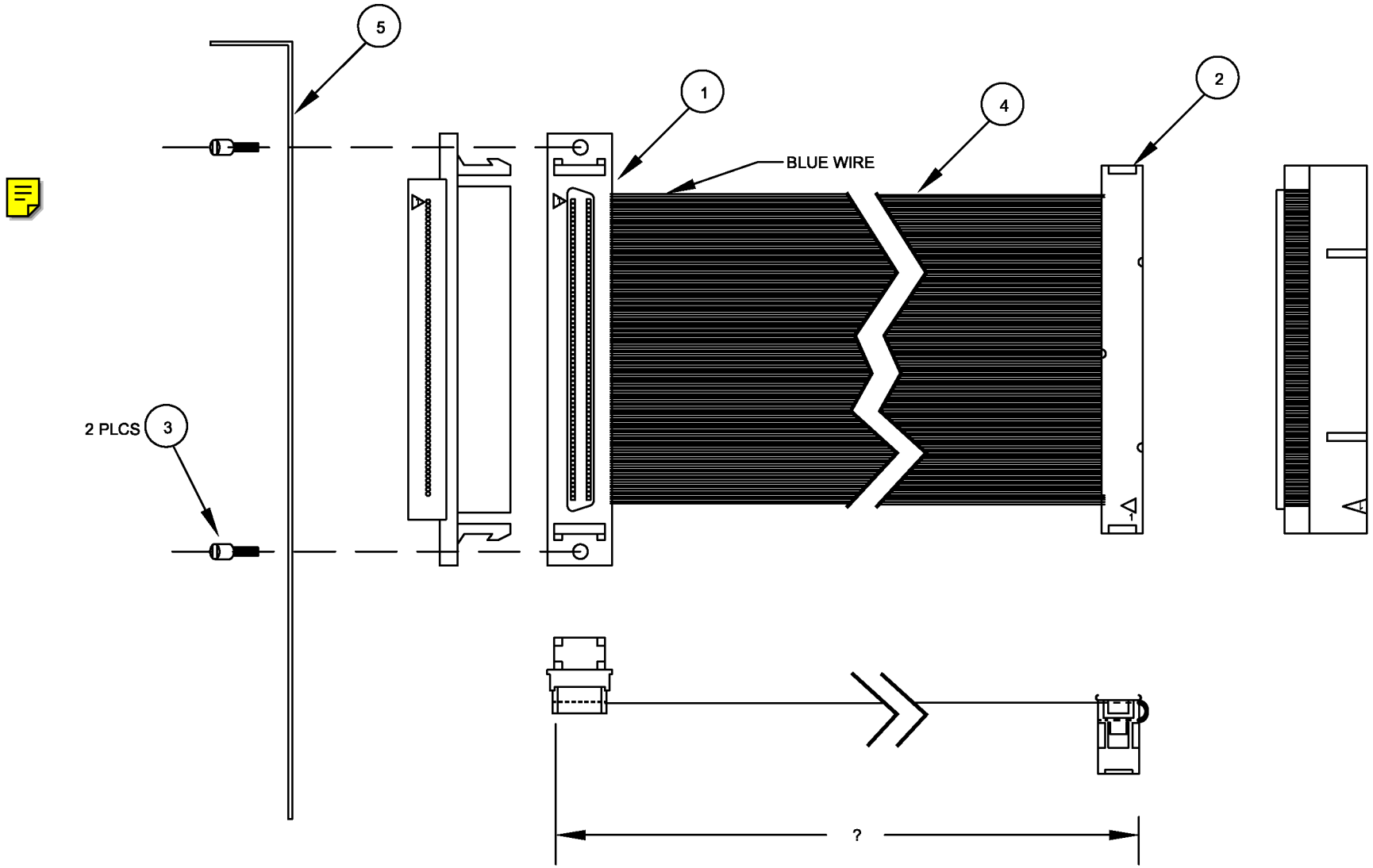
ITEM	DESCRIPTION	PART #	QUANITY
1	SCREW 2.5mm X 5mm PAN HEAD SS	8042100	8
2	SPACER 12mm/4.5mm/2.5mm ROUND SS	8680069	4

6011482

D TO A / A TO D

PCI CARD MOUNTING

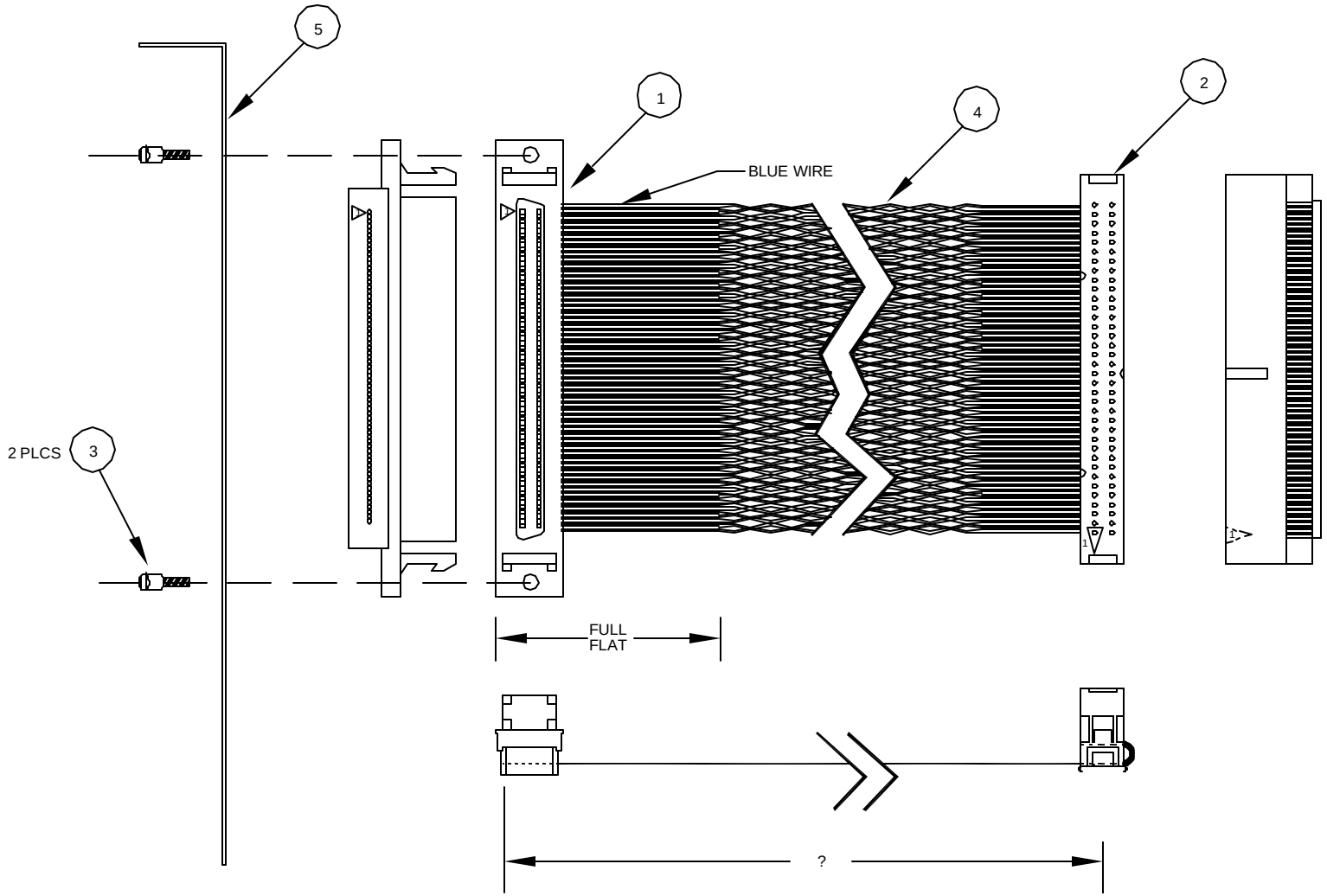
DIA. 7000226 Rev. A



NOTES: 1) LENGTH TO BE DETERMINED BY THE DASH ##'S
2) THE DASH ##'S ARE REPRESENTING THE LENGTH OF THE CABLE IN HALF INCH INCREMENTS

EXAMPLE: 1) THE PART NO: 1716XXX-02 = 1 INCH CABLE
EXAMPLE: 2) THE PART NO: 1716XXX-10 = 5 INCH CABLE
EXAMPLE: 3) THE PART NO: 1716XXX-25 = 12 1/2 INCH CABLE

USED ON	DRAWN BY B. GALAZIOS	ACROAMATICS INC.		
	DATE 6/03	TITLE	CABLE DRAWING 68S TO 68S MINI SCSI III	
	CHECKED BY			
	DATE	SIZE B	DRAWING # 1716422-XX	REV. B
	APPROVED BY	SCALE FULL	SHEET 1 OF 1	
	DATE			



NOTES: 1) LENGTH TO BE DETERMINED BY THE DASH ##'S

2) THE DASH ##'S ARE REPRESENTING THE LENGTH OF THE CABLE IN HALF INCH INCREMENTS

EXAMPLE: 1) THE PART NO: 1716XXX-02 = 1 INCH CABLE

EXAMPLE: 2) THE PART NO: 1716XXX-10 = 5 INCH CABLE

EXAMPLE: 3) THE PART NO: 1716XXX-25 = 12 1/2 INCH CABLE

USED ON	DRAWN BY B. GALAZIOS	ACROAMATICS INC.		
	DATE 8/02	TITLE CABLE DRAWING 68S TO 68S MINI SCSI III		
	CHECKED BY			
	DATE	SIZE B	DRAWING # 1716459-XX	REV. A
	APPROVED BY	SCALE FULL	SHEET 1 OF 1	
	DATE			

LIST OF MATERIALS 8176459-XX PAGE 1 OF 1

CBL 68S TO 68S MINI SCSI 3

DASH NUMBER MEASURES HALF INCHES

ASSEMBLY PN 1716459-XX DRAWN BY rjg Aug 8 11:41

REVISION A ENGINEERING APPROVAL _____ DATE _____

MANUFACTURING APPROVAL _____ DATE _____

NO.	PART NO	QNTY	DESCRIPTION	MANUFACTURERS PN	VENDOR	REFERENCE
1	6970207	1	CONN 68S MINI D-SUB	1200-068S-SCSI3	PI-MFG	
2	6970220	1	CONN CBL 68S MINI SOCKET	82068-6006	3M	
3	2794199	2	CONN SCSI STAND-OFF 2-56X1/2	786585-2	TCC-INC	
4	9800313	0	WIRE 30 AWG .025 68 COND T&F	425-3006-068(5.25)	AMPHENOL	Quantity is INCHES
5	6730131	1	FR PNL-PCI 8 STREAM	9047-8240B	GOMPF	

REV	REASON	MANDATORY	INITIATED BY	APPRV	DATE
A	RELEASE ECR 4863		BL		5/03
B	ECR# 4874		BL		6/03

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X																								

LIST OF MATERIALS 8111482-11

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1																									

PC CARD 1290238

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X																								

SCHEMATICS 2111482-11

MANUFACTURING:

VERIFY REVISION LEVELS OF WIRELIST AND L.O.M. BEFORE BUILDING CARD.

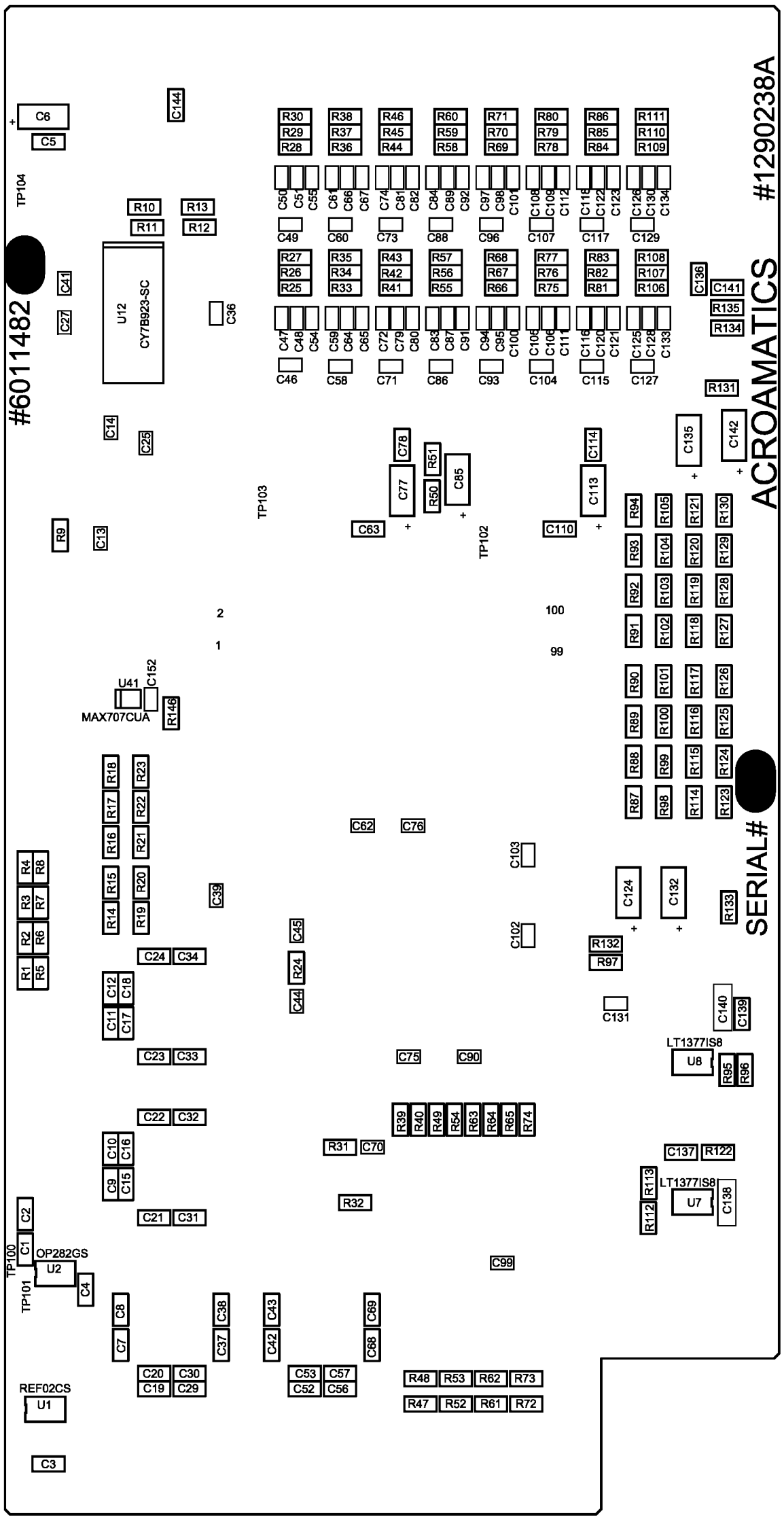
DR	B. GALAZIOS	6/03
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

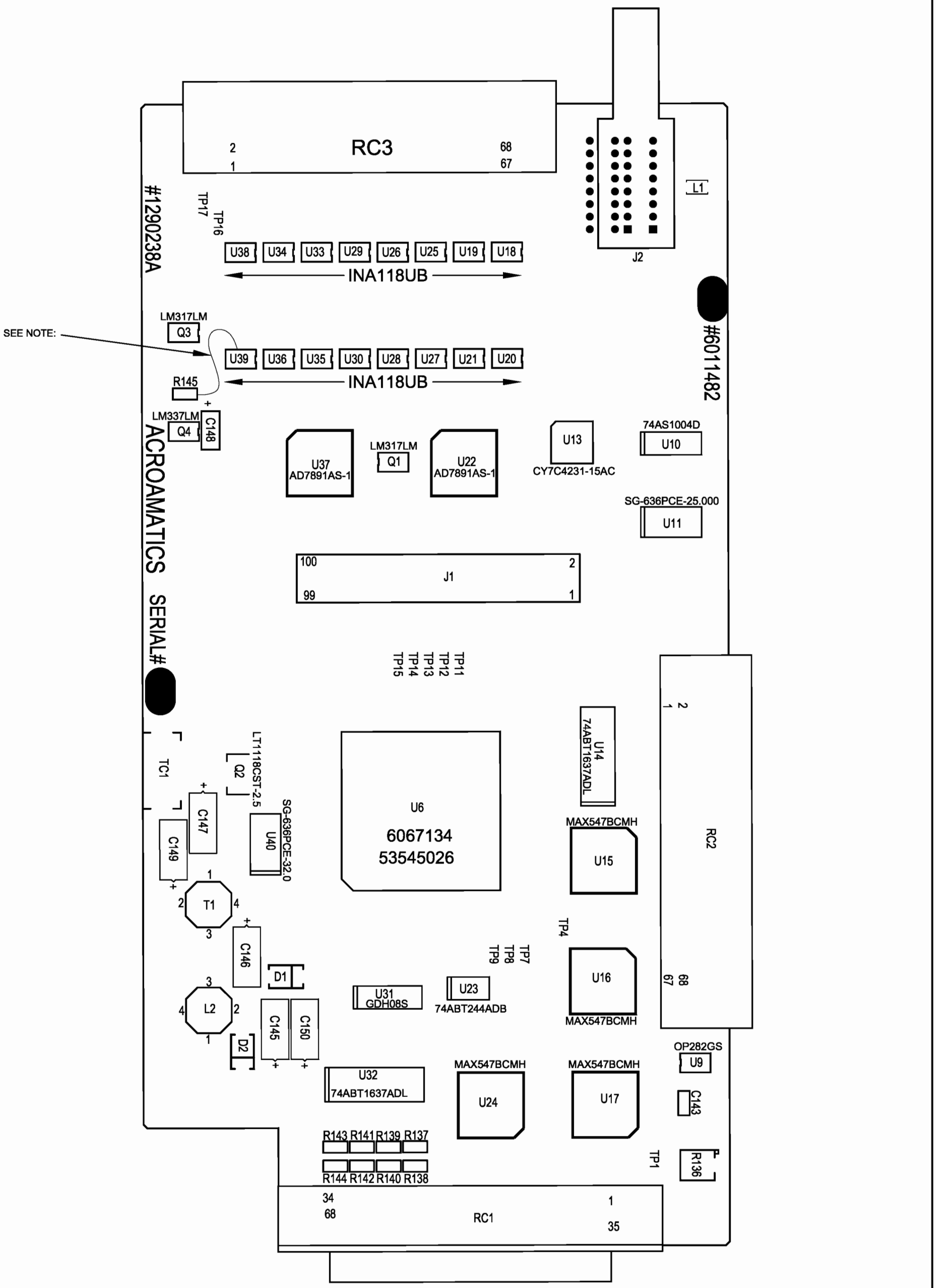
ASSEMBLY, CIRCUIT CARD

D TO A/A TO D CONVERTER MEZZ

SIZE	SCALE	DWG NO.
B	NTS	6011482-11
SHEET	1 OF 3	REV B



DR B. GALAZIOS	6/03	ACROAMATICS TELEMETRY SYSTEMS GOLETA, CAL. 93117	
CHK			
APPD		ASSEMBLY, CIRCUIT CARD D TO A/A TO D CONVERTER MEZZ	
		SIZE B	SCALE NTS	DWG NO. 6011482-11
NEXT ASSY	USED ON			
APPLICATION		SHEET 2 OF 3		REV B



NOTE: ADD WIRE ON COMPONENT SIDE FROM R145 TO U39-4

DR	B. GALAZIOS	6/03
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

D TO A/A TO D CONVERTER MEZZ

SIZE	SCALE	DWG NO.	REV
B	NTS	6011482-11	B

SHEET 3 OF 3

ACROAMATICS

TELEMETRY SYSTEMS

Engineer Bryan L.

Drawing 6011482-11 Last Used Type Standard

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
1	1290238	1	EACH	PCB D TO A/A TO D MEZZ			1290238	ACROAMATICS	
2									
3	2796120	1	EACH	CONN PC 7P HDR RTANGLE SMT			53261-0790	MOLEX	TC1
4	2796106	1	EACH	CONN PC 68P .05 SUB-D RTANGL			787082-7	AMP	RC1
5	2796129	2	EACH	CONN PC 68P MINI HDR RTANGLE			81068-560203	3M	RC3;RC2
6	2796121	1	EACH	CONN PC 100P HDR STRGHT SMT			61083-104000	BERG	J1
7									
8	1903069	45	EACH	CAP X7R .1UF 5% 50V SMT-0805			C0805C104J5RAC	KEMET	C1;C2;C3;C4;C5;C7;C8;C9 C10;C11;C12;C15;C16;C17 C18;C19;C20;C21;C22;C23 C24;C29;C30;C31;C32;C33 C34;C37;C38;C42;C43;C52 C53;C56;C57;C63;C68;C69 C78;C110;C114;C136;C141 C143;C144
9	1922656	9	EACH	CAP TA 10uF 10% 20V SMT			ECS-T1DX106R	PANASONIC	C6;C77;C85;C113;C124 C132;C135;C142;C148
	1922656A	**Acceptable Substitute**					T491B106K020AS	KEMET	
10	1903079	51	EACH	CAP X7R .022uF 10% 50V SMT-603			C0603C223K5RAC	KEMET	C13;C14;C25;C27;C36;C39;C41 C44;C45;C46;C49;C54;C55;C58 C60;C62;C65;C67;C70;C71 C73;C75;C76;C80;C82;C86 C88;C90;C91;C92;C93;C96 C99;C100;C101;C102;C103 C104;C107;C111;C112;C115 C117;C121;C123;C127;C129 C131;C133;C134;C152
11	1904106	32	EACH	CAP NPO 100pF 5% 50V SMT			ECU-V1H101JCV	PANASONIC	C47;C48;C50;C51;C59;C61 C64;C66;C72;C74;C79;C81 C83;C84;C87;C89;C94;C95 C97;C98;C105;C106;C108 C109;C116;C118;C120;C122 C125;C126;C128;C130
12									
13	1903068	2	EACH	CAP X7R 4700pF 10% 50V SMT			ECU-V1H472KBG	PANASONIC	C139;C137
14	1903073	2	EACH	CAP X7R .047uF 10% 50V SMT			ECU-V1H473KBW	PANASONIC	C140;C138
15	1922659	5	EACH	CAP TA 33uF 10% 20V SMT			593D336X9020D2T	SPRAGUE	C145;C146;C147;C149;C150
16									
17									
18	7555002	2	EACH	RECTIFIER SCHOTTKY 30V 1A SMT			MBRS130LT3(1BL3)	MOTOROLA	D1;D2
19	5250010	1	EACH	INDUCTOR 1uH .45OHM 475ma			ELJ-PC1ROMF	PANASONIC	L1
20	5250009	1	EACH	INDUCTOR DUAL 10uH SMT			CTX10-1	COILTRONICS	L2
21	7580041	1	EACH	REGULATOR +2.5V 800ma SMT			LT1118CST-2.5	LINEAR	Q2
22	7580017-01	2	EACH	REGULATOR ADJUSTABLE POS SMT			LM317LM	NATIONAL	Q3;Q1
23	7580018-01	1	EACH	REGULATOR ADJUSTABLE NEG SMT			LM337LM	NATIONAL	Q4

ACROAMATICS

TELEMETRY SYSTEMS

Engineer Bryan L.

Drawing 6011482-11 Last Used Type Standard

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
24									
25	7680981	78	EACH	RES 10K .1W 1% SMT-0805			ERJ-6ENF10.0K	PANASONIC	R1;R2;R3;R4;R5;R6;R7;R8 R14;R15;R16;R17;R18;R19 R20;R21;R22;R23;R25;R27 R29;R30;R31;R32;R33;R34 R36;R38;R39;R40;R41;R43 R44;R46;R47;R48;R49;R52 R53;R54;R55;R57;R58;R60 R61;R62;R63;R64;R65;R66 R68;R69;R71;R72;R73;R74 R75;R77;R78;R80;R81;R83 R84;R86;R106;R108;R109 R111;R133;R137-R144;R146
26	7680980	35	EACH	RES 33.2 OHM .1W 1% SMT-0805			ERJ-6ENF33.2	PANASONIC	R9;R24;R87;R88;R89;R90 R91;R92;R93;R94;R97;R98 R99;R100;R101;R102;R103 R104;R105;R114;R115;R116 R117;R118;R119;R120;R121 R123;R124;R125;R126;R127 R128;R129;R130
27	7672756	2	EACH	RES 82 OHM 1/4W 5% SMT			ERJ-14YJ820U	PANASONIC	R13;R10
28	7672757	2	EACH	RES 130 OHM 1/4W 5% SMT			ERJ-14YJ131U	PANASONIC	R11;R12
29	7680983	16	EACH	RES 100K .1W 1% SMT-0805			ERJ-6ENF100K	PANASONIC	R26;R28;R35;R37;R42;R45 R56;R59;R67;R70;R76;R79 R82;R85;R107;R110
30	7680928	3	EACH	RES 249 OHM .1W 1% SMT-0805			ERJ-6ENF249	PANASONIC	R50;R134;R145
31	7680915	1	EACH	RES 750 OHM .1W 1% SMT-0805			ERJ-6ENF750	PANASONIC	R51
32	7680936	1	EACH	RES 3.09K .1W 1% SMT-0805			ERJ-6ENF3.09K	PANASONIC	R95
33	7680991	1	EACH	RES 2.61K .1W 1% SMT-0805			ERJ-6ENF2.61K	PANASONIC	R96
34	7680937	1	EACH	RES 21.5K .1W 1% SMT-0805			ERJ-6ENF21.5K	PANASONIC	R112
35	7680925	1	EACH	RES 6.19K .1W 1% SMT-0805			ERJ-6ENF6.19K	PANASONIC	R113
36	7680990	2	EACH	RES 2K .1W 1% SMT-0805			ERJ-6ENF2.00K	PANASONIC	R132;R122
37	7680987	2	EACH	RES 1.5K .1W 1% SMT-0805			ERJ-6ENF1501	PANASONIC	R135;R131
38									
39									
40	7093057	1	EACH	4mm TRIM POT 10K 13-TURN SMT			322J-1-103E	BOURNS	R136
	7093057A	**Acceptable Substitute**					GV4JT-B-103K	TOCOS	
41	9543007	1	EACH	XFMR/INDUCTOR SMT			CTX10-2	COILTRONICS	T1
42	7580040	2	EACH	REGULATOR +5/-5V 1.5A SMT			LT1377IS8	LINEAR	U7;U8
43	6350063	1	EACH	OSCIL. XTAL 25.000MHZ SMT 3V			SG-636PCE-25.000	EPSON	U11
44	6350062	1	EACH	OSCIL. XTAL 32.000MHZ SMT 3V			SG-636PCE-32.000	EPSON	U40
45	5303021-01	1	EACH	IC REFERENCE PREC. 5V SMT			REF02CS	ANALOG-DEVICES	U1
46	5301282	2	EACH	IC DUAL OP AMP 9v/us SMT			OP282GS	ANALOG-DEVICES	U9;U2
47	5308423-15	1	EACH	IC 2Kx9 SYNCHRONOUS FIFO SMT			IDT72231L15PF	IDT	U13
	5308423-15A	**Acceptable Substitute**					CY7C4231-15AC	CYPRESS	

ACROAMATICS

TELEMETRY SYSTEMS

Engineer Bryan L.

Drawing 6011482-11 Last Used Type Standard

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
48									
49	5308119	1	EACH	IC FIBER OPTIC XMITTER 266MHZ			HFBR-1119T	AGILENT	J2
50	5302034	1	EACH	IC HEX INVERTER (SMD)			74AS1004D	TI	U10
51	5308003	1	EACH	IC 160-330MBPS SERIAL XMIT			CY7B923-SC	CYPRESS	U12
52	5300374-55	2	EACH	IC 16BIT D-F/F EDGE-TRIG SMT			74ABT16374ADL	GENERIC	U14;U37
53	5400028	4	EACH	IC 13-BIT DAC VOUT W/PARL			MAX547ACMH	MAXIM	U15;U16;U17;U24
54	5301118	16	EACH	IC INSTRUMENT AMP			INA118UB	BURR-BROWN	U18;U19;U20;U21;U25;U26 U27;U28;U29;U30;U33;U34 U35;U36;U38;U39
55	2840032	2	EACH	IC 12-BIT ADC 450KSPS PARL			AD7891AS-1	ANALOG-DEVICES	U37;U22
56	5300244-91	1	EACH	IC OCTAL BUFFER NI TS SMT			SN74ABT244ADB	GENERIC	U23
57					*				
58	6067134	1	EACH	DAC MEZZANINE INTERFACE	*	KIT	5354026-REV.B	ACROAMATICS	U6, DACM7134
59	9070015	1	EACH	DIP SWITCH 8-POS SLIDE SMT			218-8LPST	CTS	U31
	9070015A	**Acceptable Substitute**					GDH08S	AUGAT	
60	5302707	1	EACH	IC POWER UP RESET			MAX707CUA	MAXIM	U41

REV	REASON	MANDATORY	INITIATED BY	APPRV	DATE
A	RELEASE ECR 4863		BL		5/03
B	ECR# 4874		BL		6/03

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X																								

LIST OF MATERIALS 8111482-12

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1																									

PC CARD 1290238

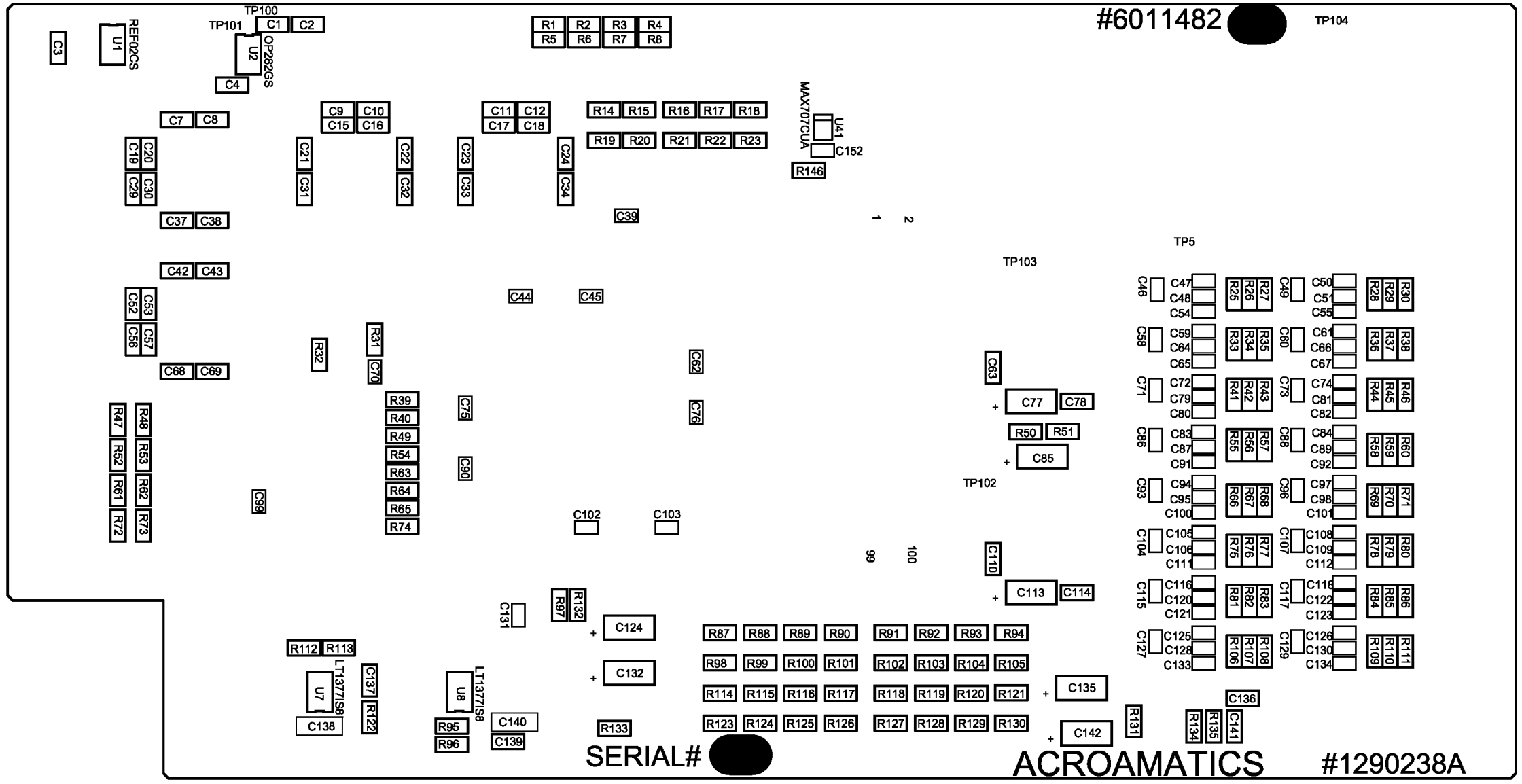
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X																								

SCHEMATICS 2111482-12

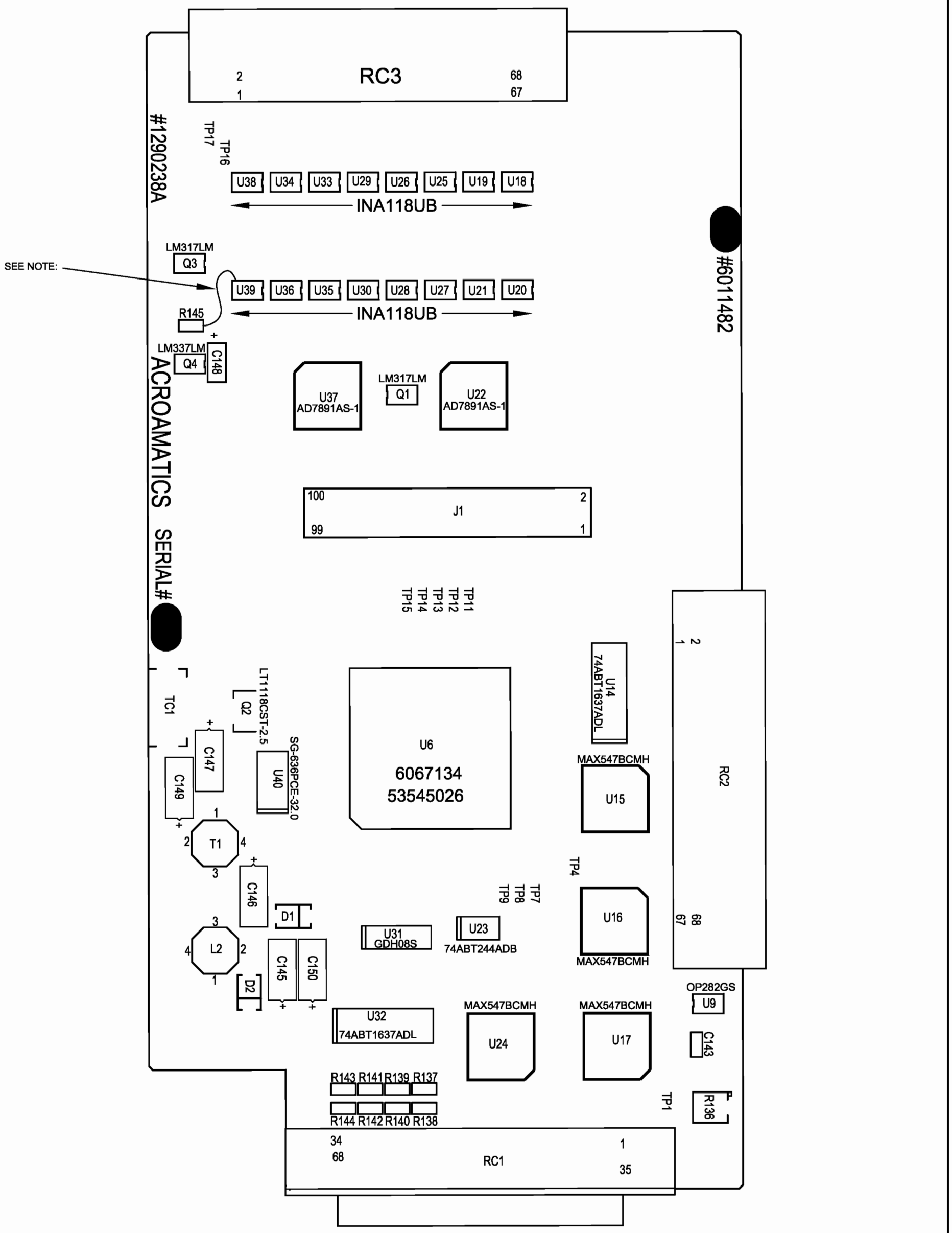
MANUFACTURING:

VERIFY REVISION LEVELS OF WIRELIST AND L.O.M. BEFORE BUILDING CARD.

DR	B. GALAZIOS	6/03	ACROAMATICS TELEMETRY SYSTEMS GOLETA, CAL. 93117
CHK			
APPD			ASSEMBLY, CIRCUIT CARD
			D TO A/A TO D CONVERTER MEZZ
NEXT ASSY	USED ON		SIZE: B / SCALE: NTS / DWG NO. 6011482-12
APPLICATION			SHEET 1 OF 3 / REV B



DR	B. GALAZIOS	6/03	ACROAMATICS	
CHK			TELEMETRY SYSTEMS GOLETA, CAL. 93117	
APPD			ASSEMBLY, CIRCUIT CARD	
			D TO A/A TO D CONVERTER MEZZ	
NEXT ASSY	USED ON		SIZE B	SCALE NTS
			DWG NO. 6011482-12	
APPLICATION			SHEET 2 OF 3	REV B



NOTE: ADD WIRE ON COMPONENT SIDE FROM R145 TO U39-4

DR	B. GALAZIOS	6/03
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

D TO A/A TO D CONVERTER MEZZ

SIZE	SCALE	DWG NO.	REV
B	NTS	6011482-12	B

SHEET 3 OF 3

ACROAMATICS

TELEMETRY SYSTEMS

Engineer Bryan L.

Drawing 6011482-11 Last Used 3/7/2006 Type Standard

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
1	1290238	1	EACH	PCB D TO A/A TO D MEZZ			1290238	ACROAMATICS	
2									
3	2796120	1	EACH	CONN PC 7P HDR RTANGLE SMT			53261-0790	MOLEX	TC1
4	2796106	1	EACH	CONN PC 68P .05 SUB-D RTANGL			787082-7	AMP	RC1
5	2796129	2	EACH	CONN PC 68P MINI HDR RTANGLE			81068-560203	3M	RC3;RC2
6	2796121	1	EACH	CONN PC 100P HDR STRGHT SMT			61083-104000	BERG	J1
7									
8	1903069	43	EACH	CAP X7R .1UF 5% 50V SMT-0805			C0805C104J5RAC	KEMET	C1;C2;C3;C4;C7;C8;C9 C10;C11;C12;C15;C16;C17 C18;C19;C20;C21;C22;C23 C24;C29;C30;C31;C32;C33 C34;C37;C38;C42;C43;C52 C53;C56;C57;C63;C68;C69 C78;C110;C114;C136;C141 C143
9	1922656	8	EACH	CAP TA 10uF 10% 20V SMT			ECS-T1DX106R	PANASONIC	C77;C85;C113;C124 C132;C135;C142;C148
	1922656A	**Acceptable Substitute**					T491B106K020AS	KEMET	
10	1903079	44	EACH	CAP X7R .022uF 10% 50V SMT-603			C0603C223K5RAC	KEMET	C39;C44;C45;C46;C49;C54;C55 C58 C60;C62;C65;C67;C70;C71 C73;C75;C76;C80;C82;C86 C88;C90;C91;C92;C93;C96 C99;C100;C101;C102;C103 C104;C107;C111;C112;C115 C117;C121;C123;C127;C129 C131;C133;C134;C152
11	1904106	32	EACH	CAP NPO 100pF 5% 50V SMT			ECU-V1H101JCV	PANASONIC	C47;C48;C50;C51;C59;C61 C64;C66;C72;C74;C79;C81 C83;C84;C87;C89;C94;C95 C97;C98;C105;C106;C108 C109;C116;C118;C120;C122 C125;C126;C128;C130
12									
13	1903068	2	EACH	CAP X7R 4700pF 10% 50V SMT			ECU-V1H472KBG	PANASONIC	C139;C137
14	1903073	2	EACH	CAP X7R .047uF 10% 50V SMT			ECU-V1H473KBW	PANASONIC	C140;C138
15	1922659	5	EACH	CAP TA 33uF 10% 20V SMT			593D336X9020D2T	SPRAGUE	C145;C146;C147;C149;C150
16									
17									
18	7555002	2	EACH	RECTIFIER SCHOTTKY 30V 1A SMT			MBRS130LT3(1BL3)	MOTOROLA	D1;D2
19					*				
20	5250009	1	EACH	INDUCTOR DUAL 10uH SMT			CTX10-1	COILTRONICS	L2
21	7580041	1	EACH	REGULATOR +2.5V 800ma SMT			LT1118CST-2.5	LINEAR	Q2
22	7580017-01	2	EACH	REGULATOR ADJUSTABLE POS SMT			LM317LM	NATIONAL	Q3;Q1
23	7580018-01	1	EACH	REGULATOR ADJUSTABLE NEG SMT			LM337LM	NATIONAL	Q4
24									

ACROAMATICS

TELEMETRY SYSTEMS

Engineer Bryan L.

Drawing 6011482-11 Last Used 3/7/2006 Type Standard

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
25	7680981	78	EACH	RES 10K .1W 1% SMT-0805			ERJ-6ENF10.0K	PANASONIC	R1;R2;R3;R4;R5;R6;R7;R8 R14;R15;R16;R17;R18;R19 R20;R21;R22;R23;R25;R27 R29;R30;R31;R32;R33;R34 R36;R38;R39;R40;R41;R43 R44;R46;R47;R48;R49;R52 R53;R54;R55;R57;R58;R60 R61;R62;R63;R64;R65;R66 R68;R69;R71;R72;R73;R74 R75;R77;R78;R80;R81;R83 R84;R86;R106;R108;R109 R111;R133;R137-R144;R146
26	7680980	33	EACH	RES 33.2 OHM .1W 1% SMT-0805			ERJ-6ENF33.2	PANASONIC	R87;R88;R89;R90 R91;R92;R93;R94;R97;R98 R99;R100;R101;R102;R103 R104;R105;R114;R115;R116 R117;R118;R119;R120;R121 R123;R124;R125;R126;R127 R128;R129;R130
27					*				
28					*				
29	7680983	16	EACH	RES 100K .1W 1% SMT-0805			ERJ-6ENF100K	PANASONIC	R26;R28;R35;R37;R42;R45 R56;R59;R67;R70;R76;R79 R82;R85;R107;R110
30	7680928	3	EACH	RES 249 OHM .1W 1% SMT-0805			ERJ-6ENF249	PANASONIC	R50;R134;R145
31	7680915	1	EACH	RES 750 OHM .1W 1% SMT-0805			ERJ-6ENF750	PANASONIC	R51
32	7680936	1	EACH	RES 3.09K .1W 1% SMT-0805			ERJ-6ENF3.09K	PANASONIC	R95
33	7680991	1	EACH	RES 2.61K .1W 1% SMT-0805			ERJ-6ENF2.61K	PANASONIC	R96
34	7680937	1	EACH	RES 21.5K .1W 1% SMT-0805			ERJ-6ENF21.5K	PANASONIC	R112
35	7680925	1	EACH	RES 6.19K .1W 1% SMT-0805			ERJ-6ENF6.19K	PANASONIC	R113
36	7680990	2	EACH	RES 2K .1W 1% SMT-0805			ERJ-6ENF2.00K	PANASONIC	R132;R122
37	7680987	2	EACH	RES 1.5K .1W 1% SMT-0805			ERJ-6ENF1501	PANASONIC	R135;R131
38									
39									
40	7093057	1	EACH	4mm TRIM POT 10K 13-TURN SMT			322J-1-103E	BOURNS	R136
	7093057A	**Acceptable Substitute**					GV4JT-B-103K	TOCOS	
41	9543007	1	EACH	XFMR/INDUCTOR SMT			CTX10-2	COILTRONICS	T1
42	7580040	2	EACH	REGULATOR +5/-5V 1.5A SMT			LT1377IS8	LINEAR	U7;U8
43					*				
44	6350062	1	EACH	OSCIL. XTAL 32.000MHZ SMT 3V			SG-636PCE-32.000	EPSON	U40
45	5303021-01	1	EACH	IC REFERENCE PREC. 5V SMT			REF02CS	ANALOG-DEVICES	U1
46	5301282	2	EACH	IC DUAL OP AMP 9v/us SMT			OP282GS	ANALOG-DEVICES	U9;U2
47					*				
48									
49					*				

ACROAMATICS
TELEMETRY SYSTEMS

Engineer Bryan L.

Drawing 6011482-11 Last Used 3/7/2006 Type Standard

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
50					*				
51					*				
52	5300374-55	2	EACH	IC 16BIT D-F/F EDGE-TRIG SMT			74ABT16374ADL	GENERIC	U14;U32
53	5400028	4	EACH	IC 13-BIT DAC VOUT W/PARL			MAX547ACMH	MAXIM	U15;U16;U17;U24
54	5301118	16	EACH	IC INSTRUMENT AMP			INA118UB	BURR-BROWN	U18;U19;U20;U21;U25;U26 U27;U28;U29;U30;U33;U34 U35;U36;U38;U39
55	2840032	2	EACH	IC 12-BIT ADC 450KSPS PARL			AD7891AS-1	ANALOG-DEVICES	U37;U22
56	5300244-91	1	EACH	IC OCTAL BUFFER NI TS SMT			SN74ABT244ADB	GENERIC	U23
57					*				
58	6067134	1	EACH	DAC MEZZANINE INTERFACE	*	KIT	5354026-REV.B	ACROAMATICS	U6, DACM7134
59	9070015	1	EACH	DIP SWITCH 8-POS SLIDE SMT			218-8LPST	CTS	U31
	9070015A	**Acceptable Substitute**					GDH08S	AUGAT	
60	5302707	1	EACH	IC POWER UP RESET			MAX707CUA	MAXIM	U41

REV	REASON	MANDATORY	INITIATED BY	APPRV	DATE
A	RELEASE ECR 4863		BL		5/03
B	ECR# 4874		BL		6/03
C	ECR# 4880		BL		6/03
N/C	ECR# 5087		BL		5/06

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X	X																							

LIST OF MATERIALS 8111482-13

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1																									

PC CARD 1290238

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X	X	X																							

SCHEMATICS 2111482-13

MANUFACTURING:

VERIFY REVISION LEVELS OF WIRELIST AND L.O.M. BEFORE BUILDING CARD.

DR	B. GALAZIOS	6/03
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

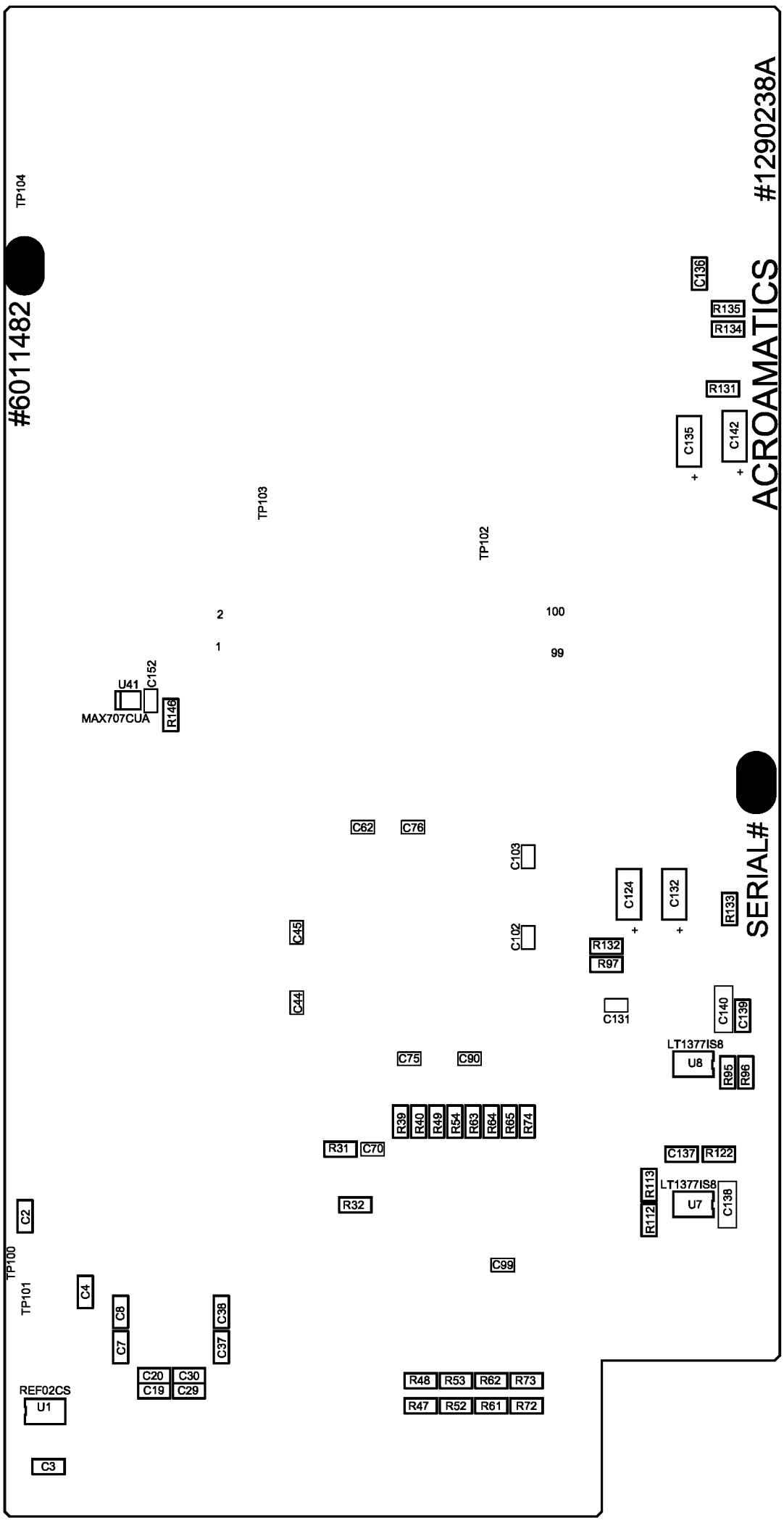
ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

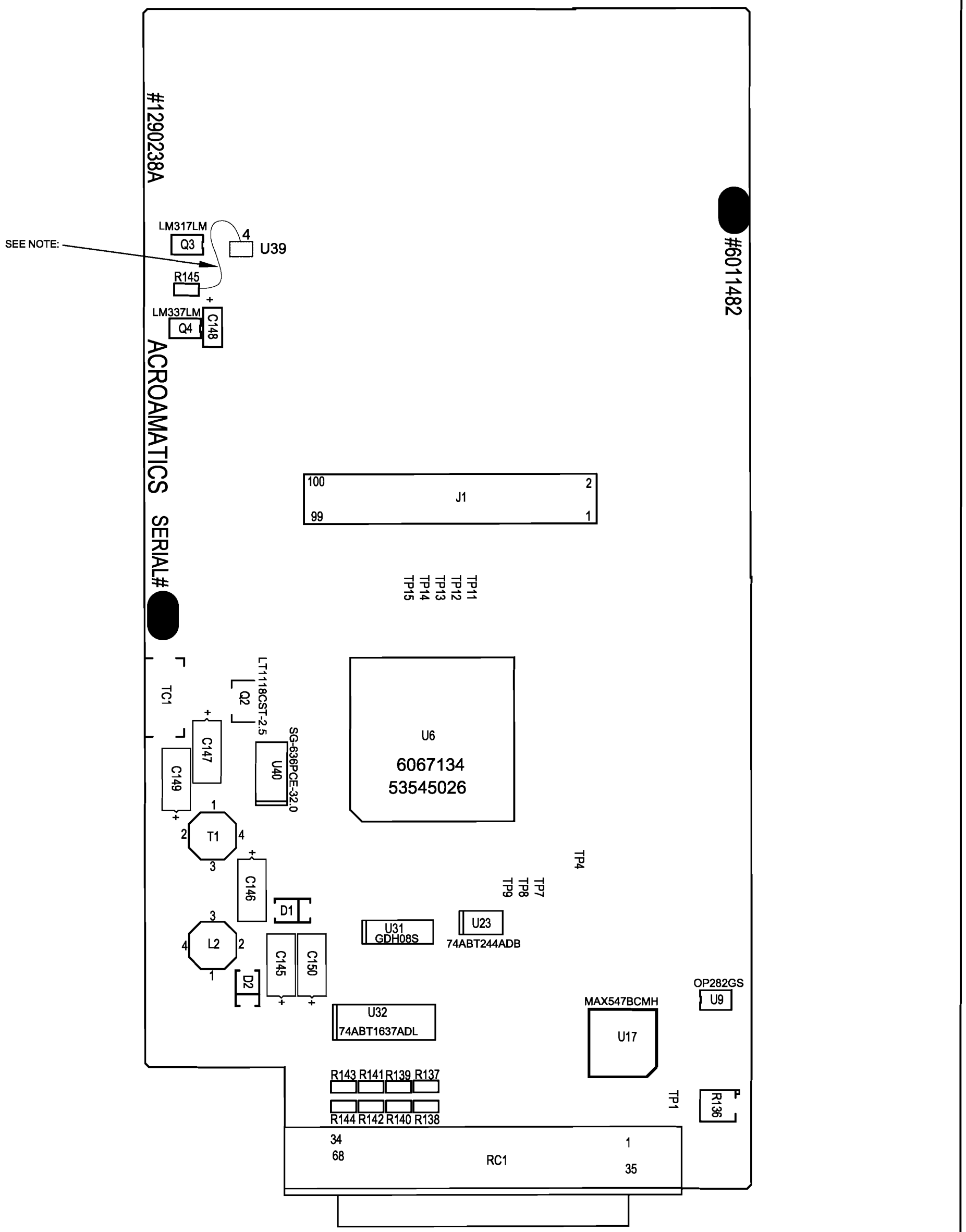
D TO A/A TO D CONVERTER MEZZ

SIZE	SCALE	DWG NO.
B	NTS	6011482-13

SHEET 1 OF 3 REV C



DR	B. GALAZIOS	6/03	ACROAMATICS TELEMETRY SYSTEMS GOLETA, CAL. 93117
CHK			
APPD			ASSEMBLY, CIRCUIT CARD D TO A/A TO D CONVERTER MEZZ
NEXT ASSY	USED ON		SIZE: B; SCALE: NTS; DWG NO. 6011482-13
APPLICATION			SHEET 2 OF 3; REV C



NOTE: ADD WIRE ON COMPONENT SIDE FROM R145
TO PAD 4 OF U39 (NOT INSTALLED)

DR B. GALAZIOS	6/03	ACROAMATICS TELEMETRY SYSTEMS GOLETA, CAL. 93117
CHK		ASSEMBLY, CIRCUIT CARD
APPD		D TO A/A TO D CONVERTER MEZZ
NEXT ASSY	USED ON	SIZE B / SCALE NTS / DWG NO. 6011482-13
APPLICATION		SHEET 3 OF 3 / REV C

ACROAMATICS

TELEMETRY SYSTEMS

Engineer Bryan L.

Drawing 6011482-13 Last Used Type Standard

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
1	1290238	1	EACH	PCB D TO A/A TO D MEZZ			1290238	ACROAMATICS	
2									
3	2796120	1	EACH	CONN PC 7P HDR RTANGLE SMT			53261-0790	MOLEX	TC1
4	2796106	1	EACH	CONN PC 68P .05 SUB-D RTANGL			787082-7	AMP	RC1
5									
6	2796121	1	EACH	CONN PC 100P HDR STRGHT SMT			61083-104000	BERG	J1
7									
8	1903069	12	EACH	CAP X7R .1UF 5% 50V SMT-0805			C0805C104J5RAC	KEMET	C2;C3;C4;C7;C8;C19;C20 C29;C30;C37;C38;C136
9	1922656	5	EACH	CAP TA 10uF 10% 20V SMT			ECS-T1DX106R	PANASONIC	C124;C132;C135;C142;C148
	1922656A	**Acceptable Substitute**					T491B106K020AS	KEMET	
10	1903079	12	EACH	CAP X7R .022uF 10% 50V SMT-603			C0603C223K5RAC	KEMET	C44;C45;C62;C70;C75;C76 C90;C99;C102;C103;C131;C152
11									
12	1903068	2	EACH	CAP X7R 4700pF 10% 50V SMT			ECU-V1H472KBG	PANASONIC	C139;C137
13	1903073	2	EACH	CAP X7R .047uF 10% 50V SMT			ECU-V1H473KBW	PANASONIC	C140;C138
14	1922659	5	EACH	CAP TA 33uF 10% 20V SMT			593D336X9020D2T	SPRAGUE	C145;C146;C147;C149;C150
15									
16									
17	7555002	2	EACH	RECTIFIER SCHOTTKY 30V 1A SMT			MBRS130LT3(1BL3)	MOTOROLA	D1;D2
18									
19	5250009	1	EACH	INDUCTOR DUAL 10uH SMT			CTX10-1	COILTRONICS	L2
20	7580041	1	EACH	REGULATOR +2.5V 800ma SMT			LT1118CST-2.5	LINEAR	Q2
21	7580017-01	1	EACH	REGULATOR ADJUSTABLE POS SMT			LM317LM	NATIONAL	Q3
22	7580018-01	1	EACH	REGULATOR ADJUSTABLE NEG SMT			LM337LM	NATIONAL	Q4
23									
24	7680981	29	EACH	RES 10K .1W 1% SMT-0805			ERJ-6ENF10.0K	PANASONIC	R31;R32;R39;R40;R47;R48 R49;R52;R53;R54;R61;R62 R63;R64;R65; R72;R73;R74 R133;R137;R138;R139 R140;R141;R142;R143 R144;R146;R148
25	7680980	1	EACH	RES 33.2 OHM .1W 1% SMT-0805			ERJ-6ENF33.2	PANASONIC	R97
26									
27									
28									
29	7680928	2	EACH	RES 249 OHM .1W 1% SMT-0805			ERJ-6ENF249	PANASONIC	R134;R145
30	7680936	1	EACH	RES 3.09K .1W 1% SMT-0805			ERJ-6ENF3.09K	PANASONIC	R95
31	7680991	1	EACH	RES 2.61K .1W 1% SMT-0805			ERJ-6ENF2.61K	PANASONIC	R96
32	7680937	1	EACH	RES 21.5K .1W 1% SMT-0805			ERJ-6ENF21.5K	PANASONIC	R112
33	7680925	1	EACH	RES 6.19K .1W 1% SMT-0805			ERJ-6ENF6.19K	PANASONIC	R113
34	7680990	2	EACH	RES 2K .1W 1% SMT-0805			ERJ-6ENF2.00K	PANASONIC	R132;R122
35	7680987	2	EACH	RES 1.5K .1W 1% SMT-0805			ERJ-6ENF1501	PANASONIC	R131;R135
36									
37									

ACROAMATICS

TELEMETRY SYSTEMS

Engineer Bryan L.

Drawing 6011482-13 Last Used Type Standard

No.	Component	Qty	U/M	Description	Rev	Type	Manufacture Part #	Manufacture	Reference
38	7093057	1	EACH	4mm TRIM POT 10K 13-TURN SMT			322J-1-103E	BOURNS	R136
	7093057A	**Acceptable Substitute**					GV4JT-B-103K	TOCOS	
39	9543007	1	EACH	XFMR/INDUCTOR SMT			CTX10-2	COILTRONICS	T1
40	7580040	2	EACH	REGULATOR +5/-5V 1.5A SMT			LT1377IS8	LINEAR	U7;U8
41									
42	6350062	1	EACH	OSCIL. XTAL 32.000MHZ SMT 3V			SG-636PCE-32.000	EPSON	U40
43	5303021-01	1	EACH	IC REFERENCE PREC. 5V SMT			REF02CS	ANALOG-DEVICES	U1
44	5301282	1	EACH	IC DUAL OP AMP 9v/us SMT			OP282GS	ANALOG-DEVICES	U9
45									
46									
47									
48									
49									
50	5300374-55	1	EACH	IC 16BIT D-F/F EDGE-TRIG SMT			74ABT16374ADL	GENERIC	U32
51	5400028	1	EACH	IC 13-BIT DAC VOUT W/PARL			MAX547ACMH	MAXIM	U17
52	5300244-91	1	EACH	IC OCTAL BUFFER NI TS SMT			SN74ABT244ADB	GENERIC	U23
53					*				
54	6067134	1	EACH	DAC MEZZANINE INTERFACE	*	KIT	5354026-REV.B	ACROAMATICS	U6, DACM7134
55	9070015	1	EACH	DIP SWITCH 8-POS SLIDE SMT			218-8LPST	CTS	U31
	9070015A	**Acceptable Substitute**					GDH08S	AUGAT	
56	5302707	1	EACH	IC POWER UP RESET			MAX707CUA	MAXIM	U41

REV	REASON	MANDATORY	INITIATED BY	APPRV	DATE
A	RELEASE ECR 4867		BL		5/03

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X																									

LIST OF MATERIALS 8111482-14

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X																									

PC CARD 1290238

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X																									

SCHEMATICS 2111482-14

MANUFACTURING:

VERIFY REVISION LEVELS OF WIRELIST AND L.O.M. BEFORE BUILDING CARD.

DR	B. GALAZIOS	5/03
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

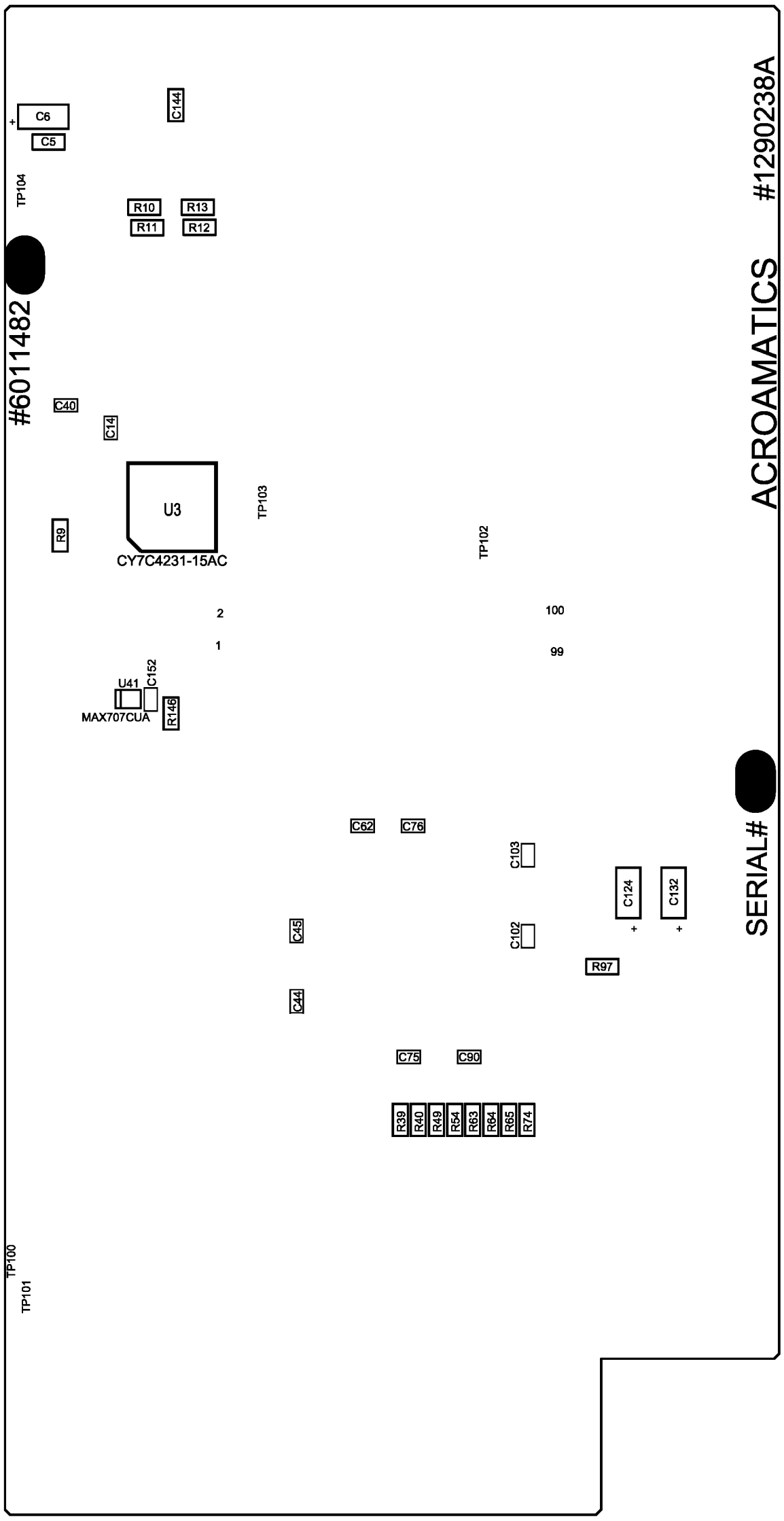
ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

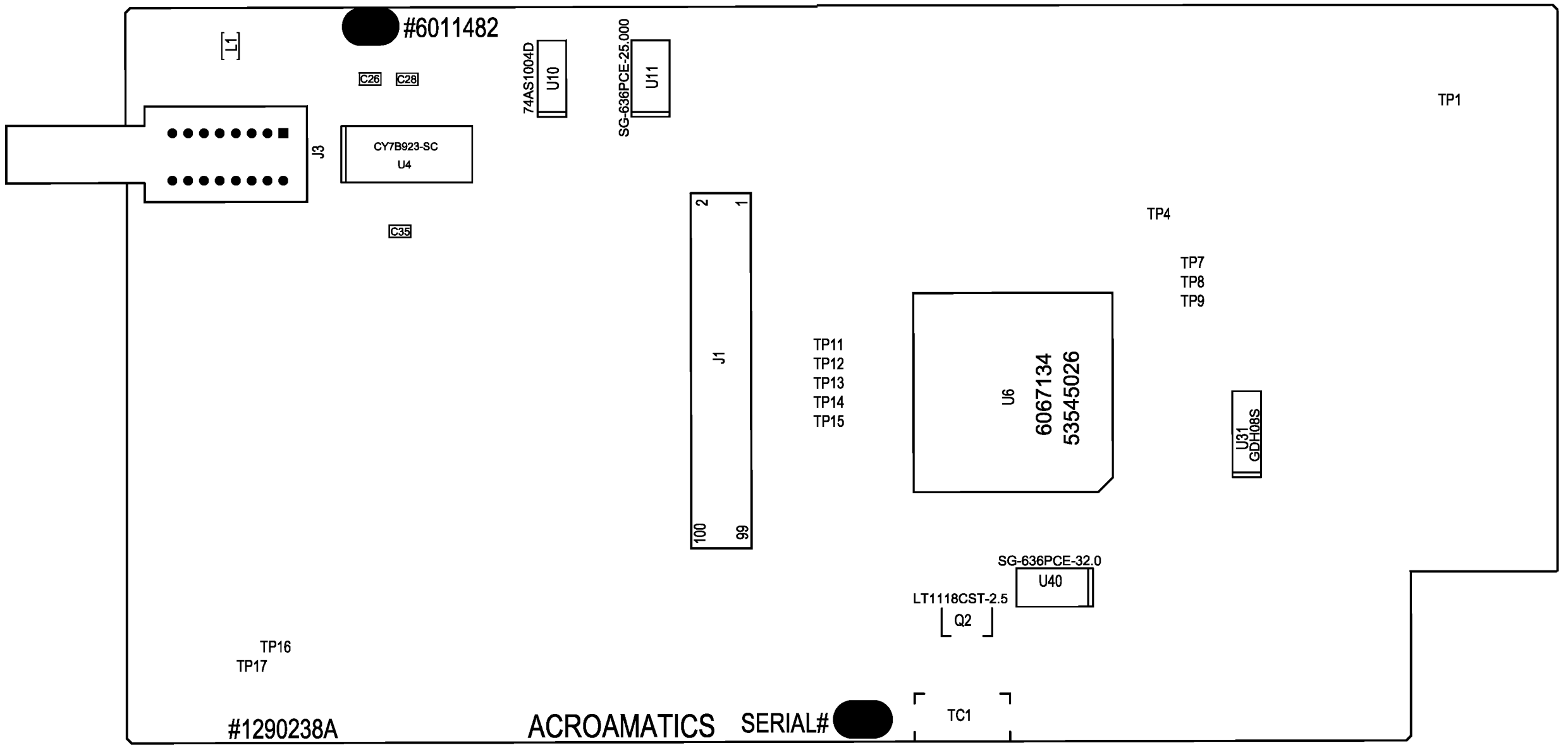
D TO A/A TO D CONVERTER MEZZ

SIZE	SCALE	DWG NO.
B	NTS	6011482-14

SHEET	REV
1 OF 3	A



DR B. GALAZIOS	5/03	ACROAMATICS TELEMETRY SYSTEMS GOLETA, CAL. 93117		
CHK		ASSEMBLY, CIRCUIT CARD D TO A/A TO D CONVERTER MEZZ		
APPD				
NEXT ASSY	USED ON	SIZE B	SCALE NTS	DWG NO. 6011482-14
APPLICATION		SHEET 2 OF 3		REV A



ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD
D TO A/A TO D CONVERTER MEZZ

DR	B. GALAZIOS	5/03					
CHK							
APPD							

SIZE	SCALE	DWG NO.	REV
B	NTS	6011482-14	A

NEXT ASSY	USED ON	SHEET
	APPLICATION	3 OF 3

REV	REASON	MANDATORY	INITIATED BY	APPRV	DATE
B	RELEASE ECR 4967		HC		5/04

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X																									

LIST OF MATERIALS 8111482-16

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1																									

PC CARD 1290238

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
X																									

SCHEMATICS 2111482-16

MANUFACTURING:

VERIFY REVISION LEVELS OF WIRELIST AND L.O.M. BEFORE BUILDING CARD.

DR	D MACDONALD	5/04
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

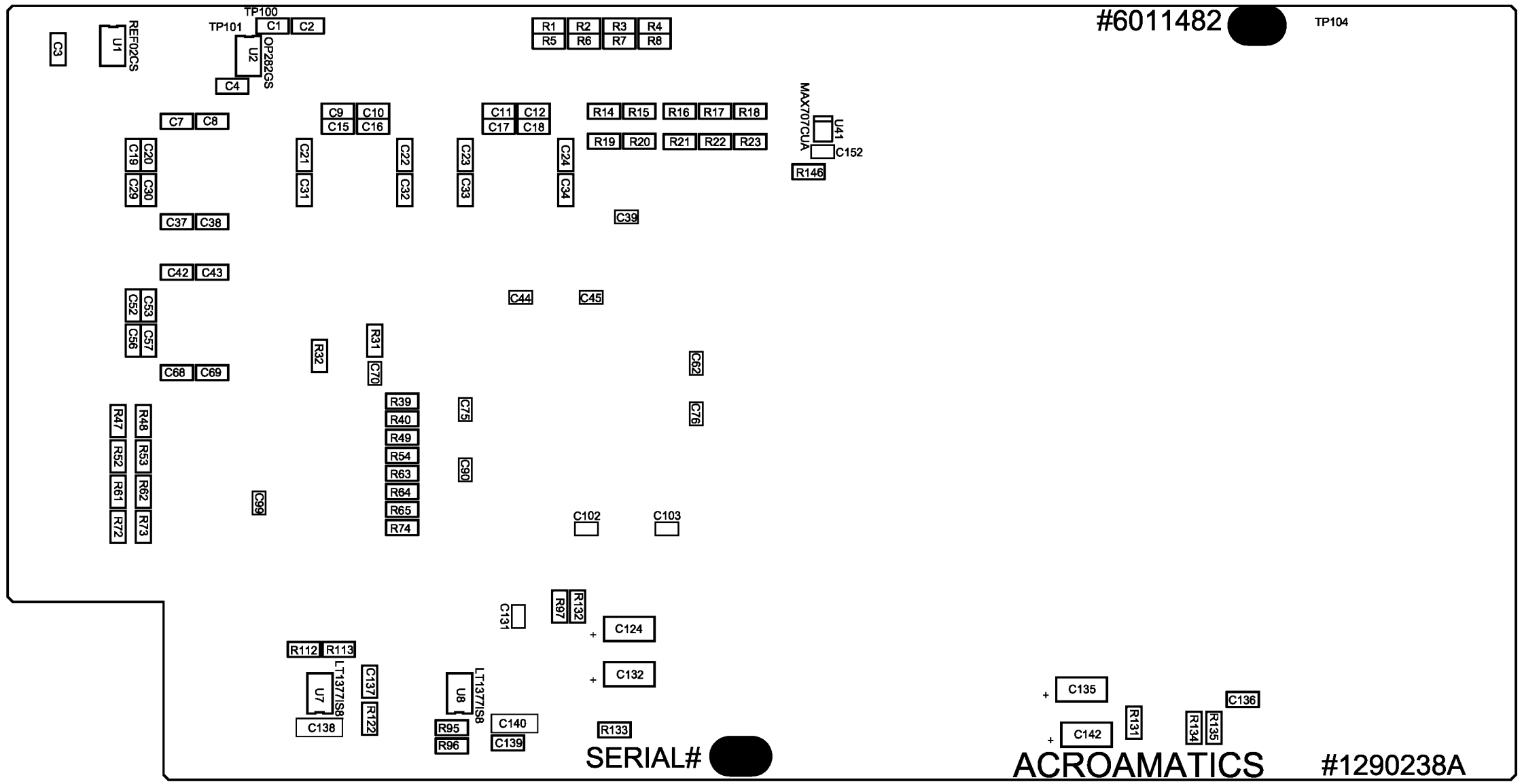
ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

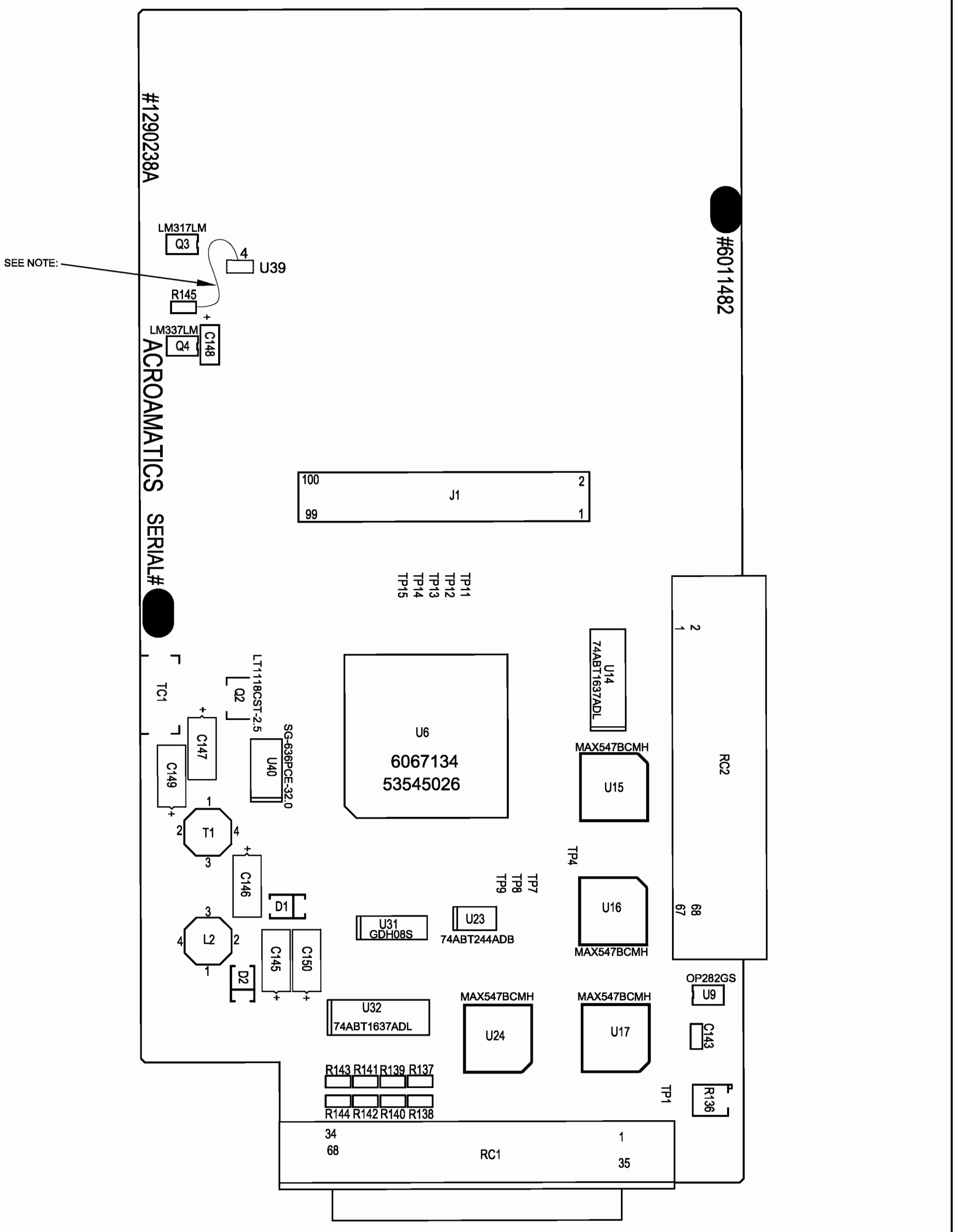
32 DAC & 32 DSC MEZZANINE CARD

SIZE	SCALE	DWG NO.
B	NTS	6011482-16

SHEET	REV
1 OF 3	B



DR	D MACDONALD	05/04	ACROAMATICS TELEMETRY SYSTEMS GOLETA, CAL. 93117
CHK			
APPD			ASSEMBLY, CIRCUIT CARD 32 DAC & 32 DSC MEZZANINE CARD
NEXT ASSY	USED ON		SIZE B / SCALE NTS / DWG NO. 6011482-16
APPLICATION			SHEET 2 OF 3 / REV B



NOTE: ADD WIRE ON COMPONENT SIDE FROM R145
TO PAD 4 OF U39 (NOT INSTALLED)

DR	D MACDONALD	6/04
CHK		
APPD		
NEXT ASSY	USED ON	
APPLICATION		

ACROAMATICS
TELEMETRY SYSTEMS
GOLETA, CAL. 93117

ASSEMBLY, CIRCUIT CARD

32 DAC & 32 DSC MEZZANINE CARD

SIZE	SCALE	DWG NO.	REV
B	NTS	6011482-16	B

SHEET 3 OF 3