

**DN 6000379
USERS MANUAL
MODEL 503VA
TIME CODE TRANSLATOR/GENERATOR**

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FEBRUARY 14, 2002

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ACROAMATICS DOCUMENT HISTORY

The following table indicates major changes made to *User's Manual Model 503VA Timecode Translator/Generator*, Acroamatics Document Number 6000379, released on February 14, 2002, and contains a record of all revisions made since that date.

DN6000379 CHANGE HISTORY			
Rev	Date	Action	Name
	02-14-02	Original Issue	DJM

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CHAPTER 1 INTRODUCTION

The Acroamatics Translator/Generator software works identically on the Model 503V VME and Model 470M PCI mezzanine cards, and this manual applies to both. You can also use the Model 470M mezzanine card with both the 502V (VME) and 1602P (PCI) versions of the Acroamatics Single Board PCM Data System.

SOFTWARE DESCRIPTION

The setup software for both the VME 503V card and the 470M VME/PCI Mezzanine card is similar to the existing Acroamatics setup compiler. The compiler is written in C programming language for portability. The setup language is compatible with that used in the earlier Acroamatics 2110 series Telemetry Data Processors. The compiler processes the setup text for the time cards and builds a simple table of setup parameters. At the end of the input, the table is transmitted essentially intact to the hardware registers. The following sections discuss the setup syntax for the Models 503V & 470M.

You enter the Generator/Translator setup from the compiler with the **TGT** command. The general form of the setup is

```
TGT
  :
  :
commands
  :
  :
END
```

Setting the Time

To set the time enter the command

```
TIME=[L]DDD:HHMM:SS[.SS]
```

The optional parameter **L** specifies a leap year. The remaining fields are as follows

DDD	represents days (1 to 3 characters).
HH	is hours (must be two characters).
MM	is minutes (must be two characters).
SS.SS	seconds and fractions of seconds (1 to 5 characters).

Any field delimited by colons may be empty, in which case it is taken to be zero.

Setting Generate Mode

To initiate Generate mode you enter the command

```
GEN [code] [rate multiplier]
```

The optional parameter *code* specifies the output IRIG time code and must be G, A, or B. If *code* is not specified IRIG B is generated. The optional parameter *rate multiplier* determines the rate at which the time code is generated. Valid rates are X.25, X.5, X1, X2, and X4. When *rate multiplier* is not specified, X1 is used.

Setting Translate Mode

You initiate the Translate mode by entering the **XLAT** command shown below. The carrier frequency (code frequency times the rate multiplier) is the default filter cutoff frequency when a filter cutoff frequency is not entered.

```
XLAT [code][Rate Multiplier][CAR][filter-cutoff-freq][INV][OUT=code]
```

The translator normally operates in *FAILSAFE* mode. In the Failsafe mode, if the input time signal is lost, time is automatically generated at the programmed rate until the input signal is regained. The input frequency must be within 5% of the programmed rate in *FAILSAFE* mode. When the **CAR** mode is selected, the card translates at the rate corresponding to the carrier it detects. The low pass filter is normally set to the highest carrier frequency that is to be translated.

The optional parameters available when setting Translate mode are

code	<i>input code - A, B, or G</i>
rate multiplier	<i>X.25, X.5, X1, X2, or X4 - for Failsafe mode</i>
filter-cutoff-freq	<i>250Hz to 400kHz - overrides the default frequency</i>
INV	<i>inverts input polarity</i>
CAR	<i>(mode - translates at the carrier rate</i>
OUT=code	<i>generates amplitude modulated IRIG A, B, or G</i>

The parameters *code* and *rate multiplier*, which specify the input IRIG time code and the carrier frequency rate multiplier, are described above in the paragraph on the **GEN** command. The parameter *filter-cutoff-freq* sets the low-pass filter cutoff frequency. The cutoff filter frequency limits are 250Hz to 400kHz, which are specified as 250 to 400000. When it is not specified, the default value is the carrier frequency (1, 10, or 100kHz) times the rate multiplier. The *INV* parameter sets the translator for an inverted signal. The *OUT=code* option is used to specify the IRIG time code output and must be specified as G, A, or B. If it is not specified, the output code is the same as the translate code.

Specifying Slow Code

The TIME cards generate a Slow Code for strip chart time annotation. The command to set the Slow Code is a two character command. There are four Slow Code rate commands available: S1 for a 1 second frame; S2 for 10 seconds; S3 for 1 minute; and S4 for a 10 minute frame. S1 is the default selection when none is specified.

CHAPTER 2 ANALOG TO DIGITAL CONVERTER PROGRAMMING

INTRODUCTION

The Analog to Digital Converter option consists of additional circuitry installed on the Model 503V (TIME) card. For the PCI system, the A to D converters are installed on the Model 482M-32 DAC/ADC card, but not on the 482M-8 eight channel card. The two LSBs of the high nibble of the TIME card signature register are used to indicate the presence of the A to D option by changing the TIME signature to 1503 hex. The analog option provides sixteen differential inputs. Each input has a differential-to-single-ended amplifier with integral sample and hold circuitry. The inputs are multiplexed to a 12 bit A to D converter with a maximum composite conversion rate of 500,000 samples per second. For the VME card, programmable sampling intervals from 16 to 500,000 samples per second are available for each input. The sampling rates are entered via sixteen registers which are an extension of the TIME card registers in A16/D16 utility space. These registers are shown below.

A to D A16 Utility Space		
Addr	Function	Mode
2E	Channel 15 Rate Set	Read/Write
↓	↓	↓
10	Channel 0 Rate Set	Read/Write

The channel rate is set by writing a 16 bit word of the following format: bits 6-0 contain a divider (from 1 to 128) that is set by entering 0 through 127; bits 7 and 11 are reserved; and bits 10-8 contain a prescaler whose values are shown in the table below.

Rate Setup Word Prescale	
Value	Clock Rate
7	16 MHz
6	4 MHz
5	1 MHz
4	250 kHz
3	50 kHz
2	10 kHz
1	2 kHz
0	Channel Disable

Bits 10, 9, and 8 in all channels default to zero at reset, disabling the channels. Bits 15-12 at address 10 (Channel 0 rate set) are reserved to set the data format in bits 13-12. The data format defaults to zero at reset. These bits are detailed in the table below.

Value	Data Format
3	Twos complement, Right justified
2	Twos complement, Left justified
1	Offset binary, Right justified
0	Offset binary, Left justified

Analog Adjustable Switches & Jumper Settings

JP1 installed enables the analog output to Distribution.

Jumpers JP2 through JP5 allow you to set bits 7-4 of the base ID for analog channels 0-15. The TDP compiler assumes the base ID is set for 1FC0, so if you use the TDP compiler's analog port setup, you should stay with the factory setting of 1FC0. The jumpers allow you to offset analog IDs in 16 channel increments; for analog expansion boards you place the blocks of 16 channels as you want within the ID space 1F00-1FF0.

Programming Analog Sampling

The setup language for the analog channels is compatible with that used in the Acroamatics 2110 series Telemetry Data Processors. The following section discusses the setup syntax.

Standard TDP syntax is used to specify the data processing. The ID field (in this case, the ID is the channel number) must include a specification of the analog sampling rate. The schematic representation is

```

ANA
  ID(rate): alg1
           ⋮
           algn
END
```

rate is the sampling rate expressed in samples per second, and should lie between 16 and 500,000. The sum of all the sampling rates per channel should not exceed 500,000. If you exceed this rate, the data is sampled as rapidly as possible, with the total number of channels sampled at about 500,000 samples per second. This adjustment is made by the hardware by reducing the sampling rate on the higher speed channels as necessary. A rate of zero disables the channel.

The ID values for the analog channels are assigned using the programmed channel numbers relative to the base of 1FC0 hex (8128); therefore, channel 0 has output ID 8128, channel 1, output ID 8129, and channel 15, output ID 8143. You may list more than one ID on a line if the processing of the data is the same.

An example of Analog Port programming is

```
ANA
OBN      |data format is offset binary
2(10000):          FL1 2%
1(2000):  3:      PAS
4(5000):  5: 6: 7:          FL1 1%
END
```

Note the unexpressed sampling rate for channels 5, 6, and 7, which are sampled at the same rate (5000) as channel 4.

You can program the analog sampling rates and the data format with the command

```
RATE [format] rate ch1 ... chn
```

rate is the sampling rate in samples per second, 16 to 500000. A rate of zero disables the channel. A list of channels *ch₁ ... ch_n* follows the rate, and all specified channels (0-15) are set to the specified rate. To use the RATE command to set the Data Format, use the options listed below. You set one format for all of the channels. If the format is not specified in the RATE command, it is not changed from its previous setting. At power up and reset, the format is offset binary, left justified.

Format Specifier	Data Format
RJA	Twos complement, Right justified
LJA	Twos complement, Left justified
RJL	Offset binary, Right justified
LJL	Offset binary, Left justified

Analog Adjustment Procedure

Two potentiometers, VR1 and VR2, provide adjustments for gain and offset of the analog inputs as a group. These are factory adjusted and normally need no further adjustment.

To set up for these adjustments, run channel 0 at 10KHz. Bend about one inch of #18 bus wire into a U shape (a paper clip will work). Insert the two ends into connector RC1 pins 19 and 37 (top two pins of 37 pin D-SUB closest to the outside corner of the board). Use a queball jumper to connect this shorting loop to ground (TP-7).

Observe the single channel display for the ID of channel 0 (usually 1FC0). The twos complement, left justified data should be at midscale with values of FFFFFFF0 and 00000000 occurring somewhat equally. If not, adjust VR2 to obtain midscale.

Next cut in half the loop at RC1 removing the short between pins 19 and 37. Leaving the ground on one pin of RC1, connect the other pin to U39 pin 5 (-5.000V) with another queball jumper. This will put channel 0 at half scale, either positive or negative depending on connections at RC1. Adjust VR1 for a reading of FFFFC000 or 00004000. Connections at RC1 may be swapped to see if the readings are symmetrical. When pin 19 is ground and pin 37 is -5.000V,

the single channel display will show 00004000, 00003FF0, 00004010 etc., and with connections swapped, the display will show FFFFC000, FFFFC010, FFFF-BFF0, etc.