

DN 6000392

**Users Manual for the
Acroamatics Bit Synchronizer
Cards**

**Acroamatics, Inc.
70 South Kellogg Avenue
Goleta, CA 93117-3476**

6/12/2007

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ACROAMATICS DOCUMENT HISTORY

The following table indicates major changes made to Users Manual for the Acroamatics Bit Synchronizer Cards, Acroamatics Document Number DN 6000392, released on February 14, 2003 and contains a record of all revisions made since that date.

DN 6000392 CHANGE HISTORY			
Rev	Date	Action	Name
	02-14-03	Original Issue	DJM
A	01-28-04	Added FSYN, BERT, remote bit syncs	MMU
B	10-06-04	Added ENET. Converted source to MS Word	MMU
C	01-07-05	Added 2650	MMU
D	07-17-06	Added 2430P	MMU
E	11-06-06	Added EXTBS_TCP_TIMEOUT_MS and BSM_POLL_INTERVAL_MS	MMU
F	06-12-07	Added 501V-2x features	MMU

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CHAPTER 1 INTRODUCTION

BIT SYNCHRONIZER CARDS

Acroamatics provides the following bit synchronizer cards:

Model 501VA VME 32 Mbps Bit Synchronizer

A VMEbus-compatible, 2U card that synchronizes all IRIG PCM codes as well as Viterbi-encoded PCM. Processes NRZ rates from 8 bps to 32 Mbps, 16 Mbps all others.

Model 1601P PCI 32 Mbps Bit Synchronizers

PCibus-compatible, full size card that synchronizes all IRIG PCM & randomized codes including Viterbi. Processes NRZ rates from 8 bps to 32 Mbps, 16 Mbps all others.

Model 472P 32 Mbps Mezzanine Bit Synchronizer

VMEbus and PCibus-compatible mezzanine card that synchronizes all IRIG PCM and randomized codes. Processes NRZ rates from 8 bps to 32 Mbps, 16 Mbps all others. The 472P card mounts on the 1502V & 1602P Frame Synchronizers, and the 1601P Bit Synchronizer.

BIT SYNCHRONIZER CHASSIS

Acroamatics also provides the following bit synchronizer chassis:

Model 2430V Dual Bit Synchronizer

A rackmount, 3.5 inch chassis containing one or two 501V VME bus bit synchronizer cards. The 2430V is remotely controllable from a PC using the Bit Sync Menu GUI, the tdp compiler program, and from the front panel by keypad entry.

Model 2430P Dual Bit Synchronizer

A rackmount, 3.5 inch chassis containing one or two 1601P PCI bus bit synchronizer cards. The 2430P is remotely controllable from a PC using the Bit Sync Menu GUI, the tdp compiler program, and from the front panel by keypad entry.

Model 2440V Multiple Bit Synchronizer

A rackmount, 12.25" chassis containing up to 16 independent VMEbus bit synchronizers. Features a flat screen display, retractable keyboard/mouse, Windows 2000™ operating system, and hard disk storage.

Model 2640P Multiple Bit Synchronizer

A rackmount 12.25" chassis containing up to 12 (6 full, 6 mezz) independent PCI bit synchronizers. Features a flat screen display, retractable keyboard/mouse, Windows 2000™ operating system, and hard disk storage.

Model 2650P Multiple Bit Synchronizer

A rackmount 12.25" chassis containing up to 12 1601P PCI bit synchronizers with capability to add up to 12 mezzanine cards, though current software supports only a total of 16 bit synchronizers. Features a flat screen display, retractable keyboard/mouse, Windows XP™ operating system, removable hard drive, CD, floppy disk, and USB for external peripherals.

SETUP & CONTROL INTERFACES

All Acroamatics bit synchronizers are setup, programmed, and controlled through two interfaces: 1) the Windows™ menu-driven graphical user interface program **BSM** (Bit Synchronizer Menu), and 2) the command line driven **tdpc** (Telemetry Data Processor Compiler).

The setup software can control multiple bit synchronizers installed in the local computer, as with the 2440V, 2640P, and 2650P Multiple Bit Synchronizer chassis, and/or bit synchronizers installed remotely in one or more 2430V or 2430P Dual Bit Synchronizer chassis. Section Two describes how the software refers to multiple bit synchronizer cards, and how it can be configured to communicate with cards installed remotely in external 2430V or 2430P chassis.

Sections Three, Four, and Five describe the programs used for setup and monitoring bit synchronizers. Section Three of this manual describes how to use the GUI program **BSM**. Section Four describes the command line driven **tdpc**. Section Five describes **BitsStat** (Bit Sync Status Display), which displays the status of all bit synchronizers in the system.

BSM and **tdpc** offer two different ways to set up your bit synchronizers. **BSM** is best for making on-the-fly changes and monitoring, while **tdpc** is convenient for downloading a canned setup. **BSM** saves setups in text files containing **tdpc** commands. Therefore, you can setup your bit synchronizers for a particular operation and save the setup as **tdpc** text. You can later use **tdpc** to load the text file as part of a batch file, or cut-and-paste it into your master setup file for all of your Acroamatics equipment, configuring the system for a given operation with a single download.

CHAPTER 2 SYSTEM CONFIGURATION

The bit sync software supports control and monitoring of multiple bit syncs. These bit syncs could be installed in the local computer, as would be the case, for example, for the 2440V, 2640P, and 2650P chassis, if the card is part of a TDP, or for 1601 cards installed in a PC. The software can also control cards installed remotely in one or more external 2430V or 2430P chassis. The software automatically detects cards installed locally, while it detects remote cards with the help of configuration parameters. This section describes how the software uses card numbers to refer to the multiple bit sync cards, and how to use configuration parameters to assign a card numbers to bit syncs installed in one or more remote 2430V or 2430P chassis.

BIT SYNC NUMBERING

The bit sync software refers to each bit sync using a *card number*. BSM and BitsStat call card number 1 "BSYN1", while tdp addresses it using the statement "BITS 1".

Local Bit Syncs

No special software configuration is necessary for bit sync cards that are installed locally on the computer's PCI or VME bus. The software can automatically detect these cards and their card numbers. The remainder of this section explains how the software assigns card numbers to these cards.

Baseboards

The card number is set by switches on the card itself. On a PCI 1601 card, the number is set by rotary switch U84. The software identifies the 1601 card with switch setting "0" as BSYN1. See Acroamatics document DN6000383 for details about the 1601 card. On a VME 501 card, the number is set by the card's A16 address, switches SW1 and SW2. Each bit sync card number has a "well-known" A16 address that is documented in Acroamatics Application Note 032. For example, BSYN1 has A16 address 6340(hex). See Acroamatics document DN6000365 for details about the 501 card.

Mezzanines

The card number of a mezzanine bit sync is determined by the card number of its baseboard. If the mezzanine is attached to a PCMD card, the mezzanine has the same card number as the PCMD. For example, the bit sync mezzanine on PCMD6 is BSYN6. If the mezzanine is attached to a 1601 PCI bit sync baseboard, the mezzanine's card number is the baseboard's card number +1. For example, a mezzanine on BSYN1 is BSYN2.

Remote Bit Syncs

For the software to recognize a remote bit sync card, one that resides in an external Model 2430 chassis, you must identify it using an entry in the file "C:\tdpsys\tdpc.cfg". This entry assigns a card number to the external card, indicates the address of the 2430 chassis as well as the card's number within the chassis (there can be up to 2 cards), and any other parameters necessary for configuring the communication port.

GPIB (IEEE-488)

The bit sync software can communicate with a remote 2430V chassis using GPIB. The 2430P does not have GPIB. To communicate with a 2430V, National Instruments' NI-488.2 software is required, which is sold with various National Instruments GPIB adapters. To map a bit sync card on GPIB, make an entry in "C:\tdpsys\tdpc.cfg" with the following form:

```
EXTBSn=GPIBi.p,u
```

n is the card number in the local system that refers to the remote card. *i* is the National Instruments GPIB interface number. *p* is the 2430V chassis' GPIB primary address. *u* is the *unit number*, the card's card number within the 2430V chassis.

For example, assume you have a dual bit sync 2430V chassis connected to GPIB adapter 0, and you have used its System Configuration Menu (press "SEL" in Status Mode to enter menu) to assign it primary address 6. To assign card numbers 3 and 4 to these remote bit syncs, you would put the following two lines in "C:\tdpsys\tdpc.cfg":

```
EXTBS3=GPIB0.6,1
EXTBS4=GPIB0.6,2
```

These remote cards would now appear as BSYN3 and BSYN4 in BSM and BitsStat, and can be addressed as "BITS 3" and "BITS 4" in tdpc. Note that the 2430V's REMOTE button must be pressed (lit) for remote communication to occur. See Acroamatics document DN6000362 for details about the 2430 bit sync chassis.

COM Port (RS232)

The bit sync software can communicate with a remote 2430 chassis (2430V and/or 2430P) using your computer's COM port. The controlling computer should connect to the 2430 using a cross-over cable (also known as a null-modem cable, transmit and receive signals must be crossed). To map a bit sync card on the COM port, make an entry in "C:\tdpsys\tdpc.cfg" with the following form:

```
EXTBSn=COMi,u [MODE=baud,pds]
```

n is the card number in the local system that refers to the remote card. *i* is the COM port number: 1 for COM1, 2 for COM2, etc... *u* is the *unit number*, the card's card number within the 2430 chassis. Next, you can optionally specify the mode of the serial communications with the **MODE=** keyword. *baud* is the baud rate, one of 9600, 19200, 38400, 57600, or 115200. *pds* is a 3 character string describing parity, number of data bits, and number of stop bits. *p* is 'N' for no parity, 'E' for even parity, or 'O' for odd parity. *d* is '7' or '8', indicating the number of data bits. *s* is '1' or '2', indicating the number of stop bits. If **MODE=** is not specified, 19200,N81 is assumed.

For example, assume you have a dual bit sync 2430 chassis connected to your computer's COM1, and you have used its System Configuration Menu (press "SEL" in Status Mode to enter menu) to configure it for 115200 baud, no parity, 8 data bits, 1 stop bit. It does not matter how the Echo parameter is set, because the bit sync software will always send a control character to disable Echo. To assign card numbers 3 and 4 to these remote bit syncs, you would put the following two lines in "C:\tdpsys\tdpc.cfg":

```
EXTBS3=COM1,1 MODE=115200,N81
EXTBS4=COM1,2 MODE=115200,N81
```

These remote cards would now appear as BSYN3 and BSYN4 in BSM and BitsStat, and can be addressed as "BITS 3" and "BITS 4" in tdpc. Note that the 2430V's REMOTE button must be pressed (lit) for remote communication to occur. The 2430P does not have a REMOTE button—it always accepts remote input. See Acroamatics document DN6000362 for details about the 2430V bit sync chassis, and DN 6000408 for details about the 2430P.

Ethernet (TCP/IP)

The bit sync software can communicate with a remote 2430 chassis (2430V or 2430P) using TCP/IP over ethernet. To map a bit sync card on ethernet, make an entry in "C:\tdpsys\tdpc.cfg" with the following form:

```
EXTBSn=TCP.a1.a2.a3.a4:6001,u
```

n is the card number in the local system that refers to the remote card. *a1.a2.a3.a4* is the 2430 chassis' IP address. **6001** is the TCP port number monitored by the 2430 chassis. *u* is the *unit number*, the addressed card's number within the 2430 chassis.

For example, to assign card numbers 3 and 4 to remote bit syncs in a 2430 chassis with IP address 192.168.55.14, you would put the following two lines in "C:\tdpsys\tdpc.cfg":

```
EXTBS3=TCP.192.168.55.14:6001,1
EXTBS4=TCP.192.168.55.14:6001,2
```

These remote cards would now appear as BSYN3 and BSYN4 in BSM and BitsStat, and can be addressed as "BITS 3" and "BITS 4" in tdpc. Note that the 2430V's REMOTE button must be pressed (lit) for remote communication to occur. The 2430P does not have a REMOTE button—it always accepts remote input.

Note that if you are controlling 2430s over a slow or unreliable network, you may need to tune the bit sync software's transaction timeout. See the section title Ethernet Transaction Timeout for details.

You must take several additional steps to setup Ethernet communication with a 2430 dual bit sync chassis. These additional steps depend on whether you are configuring a 2430V or a 2430P.

Configuring the 2430V for Ethernet

The 2430V provides Ethernet setup by way of an embedded serial-to-Ethernet converter board. Before the 2430V can receive setup from its Ethernet input, you must perform several additional steps to configure the converter board. You can find additional information in DN6000362, "System Manual for the Model 2430V VME Bit Synchronizer".

1. First, use the 2430V's front panel System Configuration menu to enable Ethernet. From Status Mode with the REMOTE button unlit, press the "SEL" button. At the "Configure:" prompt, select "Serial". At the "Enet Installed?" prompt, select "Yes". Exit the System Configuration menu by pressing the "LD1" key. This configures the 2430V's serial port (available at rear panel position J30) to receive the serial setup commands from the embedded serial-Ethernet converter.
2. On the 2430V's rear panel, cable J30 to the DB9 connector at position J31 using a cross-over cable (also called a null modem cable, transmit and receive signals are crossed). This connects the 2430's serial port to the serial side of its embedded serial-Ethernet converter.
3. Set the 2430V's IP address. This is done from your PC rather than the 2430V's front panel. Connect your PC and the 2430V to the same local area network. Run the "Remote IP Configuration" program (Ipset.exe) that is installed as part of the Bit Synchronizer Controller software. The program should automatically detect the 2430V, though it might be prevented by firewall or internet security software running on your PC. You may need to temporarily disable these while setting the 2430V's IP address. Enter the desired IP address and mask and use the default Advanced Settings. Along with the IP address and mask, this will setup the serial port on the 2430V's embedded serial-Ethernet controller to communicate with the front panel software.
4. Make an entry of the form "**EXTBS***n*=TCP.*a1.a2.a3.a4*:6001,*u*" in the PC's "C:\tdpsys\tdpc.cfg" file, as previously described in this section.

Configuring the 2430P for Ethernet

To configure a 2430P for Ethernet, use its front panel menu to set its IP address. On the Status page, click the Remote Configuration button, and then enter the IP address and mask. Then, use that IP address to make an entry of the form "**EXTBS n =TCP.a1.a2.a3.a4:6001,u**" in the PC's "C:\tdpsys\tdpc.cfg" file, as previously described in this section.

Note: "Remote IP Configuration" program (Ipset.exe) used to set the IP address for a 2430V does not work for a 2430P. Instead, set the 2430P's IP address from its front panel menu.

OTHER CONFIGURATION

This section describes other parameters that can be placed in the C:\tdpsys\tdpc.cfg file to configure the bit sync software.

Ethernet Transaction Timeout

When controlling a 2430 chassis over Ethernet (the section titled Ethernet (TCP/IP) describes Ethernet configuration), the bit sync software uses a timeout to determine whether the remote unit is responsive. Each network transaction initiated by the bit sync software must complete within the timeout, or else the unit is reported to be unresponsive. By default, this timeout is 3 seconds. On slow networks, this may be too short and the bit sync software may repeatedly report a timeout while attempting to connect. In such cases, you may adjust the timeout by adding an entry in "C:\tdpsys\tdpc.cfg" with the following form:

```
EXTBS_TCP_TIMEOUT_MS=milliseconds
```

milliseconds is the transaction timeout in milliseconds. The larger you make the transaction timeout, the greater the time lag for the bit sync software to report the unit as unresponsive, for example if the unit were powered down. On other hand, a larger timeout will make the bit sync software more tolerant to a slow or unreliable network.

For example, to override the default transaction timeout with a value of 25 seconds for all remote 2430 units controlled over Ethernet, you would add the following line to "C:\tdpsys\tdpc.cfg":

```
EXTBS_TCP_TIMEOUT_MS=25000
```

Polling Interval

In order to keep their displays up to date, the bit sync menu (BSM) and bit sync status program (BitsStat) poll the bit sync cards for their current setup and status. By default, all cards currently displayed on the screen are polled once per second. If you wish to override the default polling period, for example to reduce the amount of network bandwidth used by the bit sync software, add an entry in "C:\tdpsys\tdpc.cfg" with the following form:

```
BSM_POLL_INTERVAL_MS=milliseconds
```

For example, to poll the displayed bit sync cards once every 2 seconds, you would add the following line to "C:\tdpsys\tdpc.cfg":

```
BSM_POLL_INTERVAL_MS=2000
```

CHAPTER 3 PROGRAMMING THE BSYN UNDER WINDOWS®

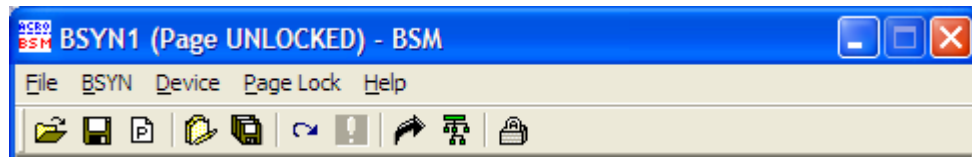
GENERAL

This section describes setup and operation of all the Acroamatics bit synchronizers, including the 501VA VME card, the 1601P full size PCI, and the 472M Mezzanine cards when running under Microsoft Windows NT, 2000, or XP. Refer to the BSYN technical manual accompanying your card for particular installation and cabling instructions.

When you install the Acroamatics software package, the icon *TM OPERATIONS* is placed on the desktop. Clicking this icon opens a folder containing the files *Bit Sync Display* and *Bit Sync Menu*. If you have also installed other Acroamatics VME or PCI cards, there will be several more files. Click on the *Bit Sync Menu* file and the GUI window shown below appears. Setup consists of entering values or making menu selections in this display. The following paragraphs describe all the selections available at this time.

PULLDOWN MENU BAR

This section summarizes the commands available on the main menu bar and tool bar.



File Menu

This menu provides items for opening and saving setups and missions, and an item for viewing the card's properties. Setups are saved with the ".bsm" extension. The ".bsm" file contains the tdpc commands that represent the setup. If you copy the contents of the ".bsm" file into a ".tdp" file, and wrap it with the BITS n and END statements, tdpc can compile it directly. A mission file has a ".tdp" extension, and can be directly compiled by tdpc. See the chapter Programming Bit Synchronizers With TDPC for more information about tdpc and its commands.

Open	Opens a saved setup (".bsm") for the currently selected BSYN.
Save	Saves currently selected BSYN's setup (".bsm").
Properties	Shows BSYN's form factor, signature, features, special codes, and I/O connection.
Open Mission	Loads setups for all installed BSYN cards from file (".tdp").
Save Mission	Save setup of all installed BSYN cards from file (".tdp").

Table 3-1: File Menu Items

BSYN Menu

Use this pulldown menu to select any individual BSYN card you want to setup. You can refresh this list using the Device→Refresh BSYN List menu item. For a discussion of card numbers, see the System Configuration chapter of this manual.

Device Menu





 Initialize BSYN	Reset the selected card, and download the default setup.
 Reconnect BSYN	Re-establishes communications with the selected card after it has reported a failure. Grayed-out under normal circumstances.
 Initialize All BSYNs	Reset and download the default setup to all BSYN cards listed in the BSYN dropdown menu.
 Refresh BSYN List	Scan for BSYN cards (local and remote) and update the list under the BSYN dropdown menu.

Table 3-2: Device Menu Items

Page Lock Menu

This menu allows you to disable menu setup for BSYN cards that you have already programmed. A page lock blocks setup from the current instance of the Bit Sync Menu only. Other BSYN setup programs (such as `tdpc.exe`, `tdpinit.exe`, or even another Bit Sync Menu instance) do not honor the menu's page locks and will operate normally. Use page locks to safeguard against unintended menu modifications to BSYNS that are in use.


 Lock Page BSYNn	Lock/Unlock the currently selected menu page.
Show All Page Locks	Open a dialog showing page lock statuses for all cards in the BSYN drop-down menu.
Lock All Pages	Lock all menu pages.
Unlock All Pages	Unlock all pages.
Preferences	Opens a dialog for setting page lock preferences. "Page Locks Persist until computer reboot" causes the page locks to be remembered even if you close and reopen the Bit Sync Menu. "Page Locks relinquished when application exits" causes the Bit Sync Menu to automatically lock the page of a card that is not idle (non-Idle status, or encoder source is XDAT/XCLK)

Table 3-3: Page Lock Menu Items

Decoder Statistics Display

Status	Amplitude	Offset	Loop Stress	Format Sync
LOCK	+00.0V	+00.0V	+00.0%	+SYN

This window section contains statistics for the selected BSYN.

Status shows IDLE (blue), LOSS (red), SEARCH (yellow), or LOCK (green) to indicate the present synchronization state of the BSYN. Amplitude displays the signal's voltage swing about its offset voltage. Offset is the signal's average offset voltage. Loop Stress indicates the input signal's percent deviation from the programmed bit rate. On BSYNs with the FSYN option, Format Sync shows the format synchronizer's status. The following table summarizes the possible values.

OFF	FSYN disabled.
LOSS	FSYN not synchronized.
SYN	FSYN is synchronized and data polarity is correct. Auto-polarity is disabled
*SYN	FSYN is synchronized, but a bit slip has occurred.
INV	FSYN is synchronized, but data is inverted. Auto-polarity is disabled.
*INV	FSYN is synchronized, but a bit slip has occurred and data is inverted. Auto-polarity is disabled.
+SYN	FSYN is synchronized and data polarity is correct. Auto-polarity is enabled.
-SYN	FSYN is synchronized, but data is inverted. Auto-polarity is enabled and has corrected the output data polarity.

Table 3-4: Format Sync Values

BERT Statistics Display (Optional)

BSYNs with the BERT option can run bit error rate tests. Activate the test and view the results from this display. The display shows different statistics depending on whether you have selected Accumulate or a test period (such as 1.0E3) for the Bert Period on the.

BERT Period Test Statistics (Optional)

BERT Stat	Current BER	Average BER	Test Counter	BERT Start/Stop
SYN	0.000E+00	0.000E+00	00000000	BERT Start/Stop

Period tests occur when you have selected a test period (like 1.0E4) for the Bert Period on the Fsyn/Bert Page. In this mode, the BSYN repeatedly samples the selected number of bits, and reports the Current BER as (# bits in error in last period) / (# bits per period). The Average BER is an average of the completed tests. The Test Counter indicates how many test samples are included in the average. Because the software samples the test results asynchronous to their completion, some tests may not be included in the average, but the software will never include the same test result more than once. BERT Start/Stop and BERT Stat are described below.

BERT Accumulation Test Statistics (Optional)

BERT Stat	Accum Errs	Avg Err/Sec	Elapsed Time	BERT Start/Stop
SYN	0.000E+00	0.000E+00	000:00:11	BERT Start/Stop

An accumulation test occurs when you have selected Accumulate for the Bert Period on the Fsyn/Bert Page. In this mode, the BSYN counts the number of errors since the start of the test and displays this value as the Accum Errs. The Elapsed Time indicates the duration of the test in the form hours:minutes:seconds. The Avg Err/Sec is (Accum Errs) / (Elapsed Time). BERT Start/Stop and BERT Stat are described below. Note that a slip during an accumulation test (*SYN, *INV) renders the error count inaccurate because bits were dropped from the test while synchronization was lost. To clear the slip condition, restart the test.

BERT Start/Stop (Optional)

Use the BERT Start/Stop button to activate a test. First select a Fsyn Src on the Fsyn/Bert Page. The BERT Start/Stop button is disabled when the Fsyn Src is Off.

BERT Stat (Optional)

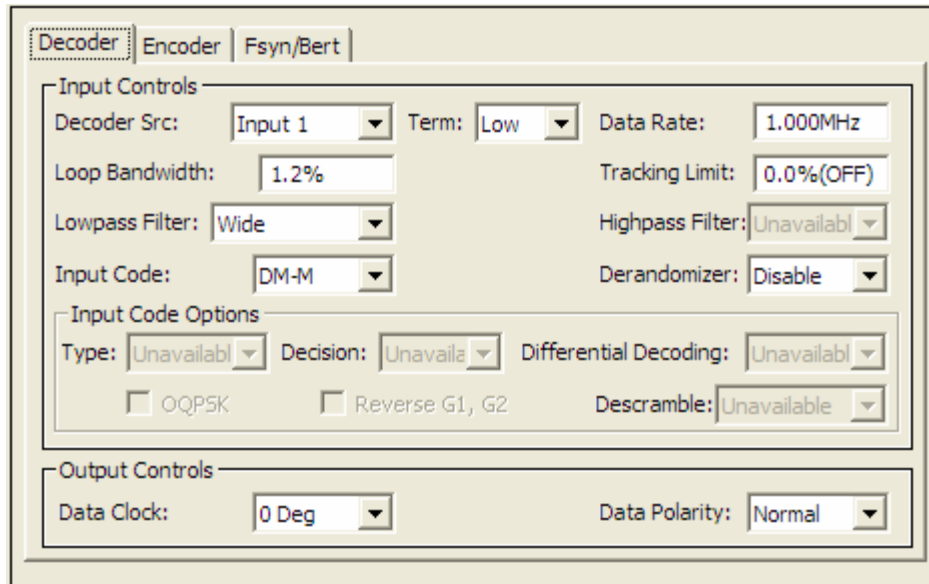
This control shows BERT synchronizer's status. It is one of the following values:

OFF	The test has been deactivated using the BERT Start/Stop button, or the Fsyn Src on the Fsyn/Bert page is Off.
OVFL	Overflow. The error counter has overflowed and the test must be restarted.
LOSS	The synchronizer is searching for the expected format.
*SYN	Synchronizer is currently locked to the expected format, but slipped during the last test period causing an indeterminate number of bits to be dropped from the test.
*INV	Synchronizer is currently locked to the expected format, but the data is inverted. Also, a bit slip during the last test period caused an indeterminate number of bits to be dropped from the test.
SYN	Synchronizer is locked to the expected format.
INV	Synchronizer is locked to the expected format, but the data is inverted.

Table 3-5: BERT Stat Values

DECODER Page

Use this section to setup your BSYN parameters to synchronize to the incoming PCM stream. Some menu selections in one field will activate or deactivate other parameter menus, depending upon whether the secondary parameters do or do not apply.



Decoder Src

Use the pulldown menu to select an input source. Different types of BSYN cards have different capabilities. The menu will detect the card type and display the appropriate options. The possible decoder sources are summarized below.

Sim(P2)	An internal path for a simulator input. The presence of this option means only that the path exists, not that a simulator is installed in your system. On VME systems, extra chassis wiring is required. Check your system documentation to find out if you have a simulator and if it is configured for this option.
Input 1-4	General purpose inputs. Mezzanines have only Input 1 (single-ended) and Input 2 (differential). VME baseboards have jumpers that allow you to configure each of the 4 inputs for either single-ended or differential. PCI baseboards have Inputs 1-3 as single-ended, and Input 4 as differential.
XCLK/XDAT	This option allows you to bypass the bitsync, and send clock and data directly to the PCM decoder.

Table 3-6: Decoder Src Choices

Term

The best termination value is dependent upon several factors that together determine the characteristic impedance of the BSYN input line. These factors include cable length, connector impedance, corrosion, etc. Use the pulldown menu to select either Low or High impedance. The settings signify 75Ω and 10KΩ terminations, respectively, for single-ended inputs or 125Ω and 10KΩ terminations, respectively, for differential inputs.

Data Rate

The BSYN remains in the IDLE state until you enter a bit rate and select an input. The BSYN then goes into SEARCH mode and begins processing input signals. Entering a rate of zero or disabling the input returns the BSYN to the IDLE state.

Enter a bit rate by moving the cursor to the Rate window and typing in the significant digits followed by k for KHz, m for MHz, and nothing for Hz. For example, typing 10.3m, 10.3MHz, 10.300m, 10300000, or 10300k and hitting <enter> will all enter and display 10.30MHz.

Loop Width

Loop width expresses the effective size of the "window" in which the bit sync can lock onto and track a signal. The larger the window, the more quickly lock is achieved, but also the more susceptible the device is to signal perturbations. The larger the numeric value of the loop width parameter is, the larger the window. The BSYN provides 32 loop widths from 0.1% to 3.2%. To enter a value, simply highlight the window and enter any value between .1 and 3.2. To enter the value, press <enter>, or shift input focus to another control.

Tracking Limit

Tracking Limit (also known as Loop Tracking) sets the maximum allowable PLL frequency deviation from the programmed bit rate. The larger the loop tracking value is, the larger the deviation range. Setting the loop tracking to 0.0% disables loop tracking; it allows the loop to track over its maximum range. The PLL is momentarily reset when the output frequency drifts beyond the % value. The BSYN card provides 100 incremental 0.1% settings from 0.0% to 9.9%. To enter the value, press <enter>, or shift input focus to another control.

Lowpass Filter

Select NARROW or WIDE bandwidth for the low-pass filter. Generally speaking, the low-pass filter removes noise and perturbations above the BSYN's frequency setting, and the high-pass filter removes signal content below the frequency setting. Using the filters does not necessarily result in better data output, and you should experiment with the filters on noisy signals or tapes. Try the over-filtered selection when your data is severely over-filtered. This selection modifies the AGC routine to compensate for the varying amplitude levels of overfiltered signals. The detection circuitry also monitors the data peaks rather than the zero crossings on bit rates above 100kbps, allowing you to recover extremely over-filtered data.

Highpass Filter

You can set the high pass filter only when you have selected a bi-phase Input Code. Select either disable or enable. See the Lowpass Filter section for a discussion of filter usage.

Input Code

Specify the input code type you want to process by entering one of the mnemonics shown in the pulldown menu. The BSYN supports the following standard PCM codes:

NRZ-L	Non-Return-to-Zero Level
NRZ-M	Non-Return-to-Zero Mark
NRZ-S	Non-Return-to-Zero Space
BiP-L	Bi-phase Level (Split Phase)
BiP-M	Bi-phase Mark
BiP-S	Bi-phase Space
DBi-M	Differential Bi-phase Mark
DBi-S	Differential Bi-phase Space
DM-M	Delay Modulation Mark (Miller)
DM-S	Delay Modulation Space (Miller)
M2-M	Modified Delay Modulation Mark (Miller)
M2-S	Modified Delay Modulation Space (Miller)
RZ	Return-to-Zero

Table 3-7: Standard Input Code Choices

The derandomizer can be applied to any input code using the Derandomizer drop down list. Decode one of the IRIG standard RNRZ codes by selecting NRZ-L for the input code, and the appropriate run length for the Derandomizer. You can also derandomize a non-standard combination, such as randomized BiP-L, in a similar fashion.

The BSYN also supports *special codes* such as Viterbi, or QPSK codes like QNZL and QNZS. Special codes are optional and will not appear in the Input Code list unless installed on the card. Some special codes have options that you set in the Input Code Options section.

Derandomizer

You can apply an IRIG derandomizer to the data after the input code conversion. Use the Derandomizer pulldown menu to select an F (forward) or R (reverse) pattern direction. Run

length values are 9, 11, 15, 17, or 23. You need to specify the run length only if you have a randomized code. If you do not specify a derandomizer length, the derandomizer is disabled.

Input Code Options

Input Code Options are activated as necessary when you select a special code as your Input Code. While the following sections discuss Viterbi, some of the controls apply to other special codes as well. The menu will enable the controls appropriate for the selected special code.

Viterbi Decoding (Optional)

The most commonly used special code is Viterbi. Activate it by selecting Viterbi from the Input Code pulldown menu. The menu presents this selection only when your BSYN has the option. The Viterbi option is not available in all BSYN card form factors.

The BSYN, when equipped with the Viterbi option, decodes data that has been encoded with a $K = 7$, rate 1/2 convolutional, forward error correcting device. This encoding applies two separate polynomials to seven consecutive bits of data, then forwards the output as two symbols, each symbol being the result of one of the polynomials. The symbol rate is therefore twice the input data rate. The symbols may be transmitted serially using time division multiplexing techniques, or in parallel, using two links (such as a QPSK modulator). Using a history of previous symbols and a maximum-likelihood decoding algorithm, the decoder recombines and processes the symbols to reproduce the original data.

Viterbi Decoder Type (Optional)

The input type can be **Serial**, with the two symbols alternating in time, or parallel. Decoding parallel inputs with the symbols simultaneously processed requires two BSYNs. One BSYN, designated the Slave, produces a soft bit decision and sends it to the other BSYN, designated the Master. The Viterbi decoder on the master BSYN takes the soft bit decisions for the two symbols and processes them to reproduce the original data. Ext SBD allows you to output the soft bit decisions to an external decoder.

Viterbi Decoder Decision (Optional)

The Viterbi decoder is optimally set to process Soft Bit decisions, in which 3 bits are used to represent one of 8 possible values in order to express not only the binary value of a bit, but also a level of confidence with respect to that value. When processing Hard Bit decisions, the decoder is provided only a single bit value of the symbol, that being either a 0 or 1. The confidence levels of the soft bit decision mode allow the Viterbi decoder to achieve a significantly higher coding gain than when decoding in hard bit decision mode. The hard bit mode is used primarily for reference purposes. Older versions of VME BSYN cards only support soft bit decisions.

Viterbi Decoder Differential Decoding (Optional)

Select Off for NRZ-L, or On for NRZ-M.

Viterbi Decoder Descramble (Optional)

In order to increase the number of binary transitions in a convolutionally encoded data stream, the data may be enhanced with a scrambling algorithm.

The BSYN supports three scrambling algorithms commonly used with convolutionally encoded data. These are the CCITT.V.35 algorithm, the INTELSAT algorithm, and G2 inversion - which simply inverts the G2 symbol generated by the convolutional encoder. Not all BSYN card types support all descramblers. The menu lists only the ones supported by your card.

Viterbi Decoder Rev G1, G2 (Optional)

Selecting this checkbox reverses the orientation of G1 and G2. For serial input, this means that G2 precedes G1 in time. For parallel input, this means that the relationship between the G1, G2 symbols, and the master, slave bit synchronizers is reversed. Not all card types support this option. The menu grays it out when it is not supported.

Viterbi Decoder OQPSK (Optional)

Selecting this checkbox allows the decoder to process OQPSK data, which is when the two parallel input symbols are staggered a 1/2 bit period. Not all card types support this option, so the menu grays it out when it is not available.

Data Clock

The decoded NRZ-L data and a synchronous clock are available at the DATA and CLCK outputs. The phase relationship between the clock and data is selectable as 0, 90, 180, or 270, expressing the phase shift in degrees between the positive transition of the output clock with respect to the start of the bit period. Most processing equipment requires either the 0 degree setting or the 180 degree setting. The remaining two selections may be used to restore clock/data pair timing which may have been skewed on a data link by uneven or long cable lengths.

Data Polarity

Select Normal or Invert to control the polarity of the decoded NRZ-L data at the DATA output.

ENCODER Page

Use this section re-encode clock and data for down stream processing, or to generate a test pattern for link testing.

The screenshot shows a software interface for the Encoder section. At the top, there are tabs for 'Decoder', 'Encoder', and 'Fsyn/Bert', with 'Encoder' selected. The interface is divided into three main sections:

- Input Controls:** Contains 'Encoder Src' (dropdown menu set to 'Decoder'), 'External Clock' (dropdown menu set to 'Unavailable'), 'Encoder Polarity' (dropdown menu set to 'Normal'), and 'Test Gen Clock' (two dropdown menus, both set to 'Unavailable').
- Outputs Controls:** Contains 'RNRZ Out' (dropdown menu set to 'Pass Thru'), 'TAPE Out' (dropdown menu set to 'NRZ-L'), 'Rand TAPE' (checkbox), 'TAPE Attenuate(dB)' (text input set to '00.0'), 'CODE Out' (dropdown menu set to 'Tape'), 'Rand CODE' (checkbox), and 'CKX2 Out' (dropdown menu set to 'x2 0 Deg').
- CODE Out Options:** Contains 'Type' (dropdown menu set to 'Unavailabl'), 'Differential Encoding' (dropdown menu set to 'Unavailabl'), 'OQPSK' (checkbox), 'Reverse G1, G2' (checkbox), and 'Scramble' (dropdown menu set to 'Unavailable').

Encoder Src

The encoder can use the clock and data recovered from BSYN's Decoder section, an external clock and data source connected via the XCLK/XDAT inputs, or a test pattern generated by the BSYN's Test Generator. For data connected via the XCLK/XDAT, you need to specify the type of External Clock. Similarly, for Test Generator data, you need to specify the Test Generator Clock. By default, the Test Generator generates a PN11F pattern. If you have the FSYN or BERT options, you can change this using the Pattern drop-down on the Fsyn/Bert page.

External Clock

Set this when the Encoder Src is XCLK/XDAT. Pulldown selections are x1 or x2, 0 or 180 degrees, corresponding to an external clock that is the bit rate or twice the bit rate, respectively. The 0 or 180 degrees indicates whether the external clock is to be inverted or non-inverted, respectively. If the rising edges of the clock coincide with the transitions of the data, the sign must be 0. If the falling edges of the clock coincide with the transitions of the data, the sign must be 180.

Encoder Data Polarity

Use this control to flip the Encoder Src data polarity.

Test Gen Clock

Specify this when the Encoder Src is Test Generator.

If you select PLL, the test generator will be clocked using the decoder section's PLL. Select the Test Generator's clock rate by entering a value into the Data Rate control on the Decoder Page. While this allows the Test Generator to generate arbitrary data rates, you should not try to use it at the same time you are using the decoder. If you are using the decoder, use a different Test Generator Clock.

If you select External, the test generator will clock its data pattern using the clock you provide at the XCLK input. The test generator will treat it as a x1 clock.

The test generator also has its own built-in rate generator. To use it as the clock source, select one of the listed bit rates (1.00E6, for example).

Starting with card version 3 of the 501VA-22 (viewable in the File→Properties dialog), cards equipped with the BERT option have a programmable frequency synthesizer. Select Synthesize from the Test Gen Clock dropdown list, and then enter the desired rate in the neighboring textbox. You can enter the rate using many different forms, including scientific notation or engineering units. When using engineering units, specify k for KHz, m for MHz, or nothing for Hz. The frequency synthesizer has tuning resolution better than 0.002%, but most rates are not exactly obtainable. After typing the desired rate, press <enter>, and the menu will set and display the nearest obtainable rate. For example, typing 1e5, or 100k, or 100000 and pressing <enter> will cause the menu to set and display a synthesized clock rate of 99.9999KHz.

RNRZ Out

This selects the randomizer's run length, 9, 11, 15, 17, or 23, and pattern direction, R (reverse) or F (forward). The randomized Encoder Src data is always available at the RNRZ-L output. If you select Disable (pass through), then data at the RNRZ output is unrandomized NRZ-L and checking Rand TAPE or Rand CODE has no effect.

Tape Out

Selects the PCM encoding available at the TAPE output. The available codes are the same as listed in the Input Code section. The randomizer is set separately from the PCM code. To randomize a PCM code at the TAPE output, just check Rand TAPE and select the run length using the RNRZ Out control.

Rand TAPE

This controls whether or not the encoded data at the TAPE out is randomized.

TAPE Attenuate(dB)

Starting with card version 3 of the 501VA-22 (viewable in the File→Properties dialog), cards equipped with the BERT option can attenuate the signal amplitude at the TAPE output. Attenuations from 0-25.5dB in 0.1dB steps are allowed. TAPE Attenuation can be used, for example, in BER testing by first setting TAPE attenuation to 0 dB and adjusting your noise level to obtain a starting signal-to-noise ratio. You can then obtain other signal-to-noise ratios by leaving the noise level fixed, and simply adjusting the Tape Attenuation. For example, if you measure your signal-to-noise ratio to be 12dB when the Tape Attenuation is set to 0dB, changing the Tape Attenuation to 1dB would give a signal-to-noise ratio of 11dB, Tape Attenuation of 2dB would give a signal-to-noise ratio of 10 dB, 3dB gives 9dB, etc.

CODE Out

This selects the data available at the CODE output. If you select Tape, the CODE output provides a TTL version of the PCM encoded data available at the TAPE output. If you select Data, the CODE output passes the Encoder Src data, and you can choose to randomize it by checking the Rand CODE checkbox.

The BSYN also supports *special codes* such as Viterbi, and QPSK codes like QNZL and QNZS. Only the special codes you have purchased will appear in the list. Some special codes have options that you set in the CODE Out Options section.

Rand CODE

This allows you to randomize the Encoder Src data at the CODE output when you have selected Data for the CODE Out control. This feature is available on Upgrade 2 BSYNs only. Check features using File→Properties.

CKX2 Out

The CKX2 pulldown menu allows you to specify the multiplier and polarity of the CKX2 output clock relative to the encoder's output data.

CODE Out Options

CODE Out Options are activated as necessary when you select a special code as your CODE Out code. While the following sections discuss Viterbi, some of the controls apply to other special codes as well. The menu will enable the controls appropriate for the selected special code.

Viterbi Encoding (Optional)

The Viterbi Encoder menu is activated when you select Viterbi from the CODE Out list. The Viterbi option provides rate 1/2, k=7 convolutional (Viterbi) encoding. The convolutionally encoded data is provided at the encoder's CODE and RNRZ connectors.

Viterbi Encoder Type (Optional)

The output type can be Serial (with the two symbols alternating in time) or Parallel, with the G1 and G2 symbols output simultaneously. Serial data is provided at the CODE connector, while parallel data is provided with the G1 symbol at the CODE connector and the G2 symbol at the RNRZ connector.

Viterbi Encoder Differential Encoding (Optional)

Select Off for NRZ-L, or On for differential NRZ-M.

Viterbi Encoder OQPSK (Optional)

For parallel output, selecting this checkbox causes the encoder to output the two symbols staggered by a half-bit period. Not all card types support this option. The menu grays it out when it is not supported.

Viterbi Encoder Reverse G1, G2 (Optional)

Selecting this checkbox reverses the orientation of G1 and G2. For serial output, this means that G2 precedes G1 in time. For parallel output, this means that G1 is provided at the RNRZ connector, while G2 is provided at the CODE connector. Not all card types support this option, so the menu grays it out when it is not available.

Viterbi Encoder Scramble (Optional)

You can use the CCITTV.35 algorithm, the INTELSAT algorithm, or G2 inversion, which simply inverts the G2 symbol generated by the convolutional encoder. Older BSYN cards do not support all scrambler types. The menu only presents a selection of those supported by your card.

Fsyn/Bert Page (Optional)

The Fsyn/Bert Page allows setup of the BSYN's FSYN and BERT features. This setup page is displayed only when the BSYN is equipped with at least one of the FSYN or BERT options.

Pattern(Optional)

This selects the pattern generated by the Test Generator, and when the FSYN option is present, the pattern expected by the Format Synchronizer. The available choices depend upon whether you have the FSYN option, the BERT option, or both. If you have neither, the Test Generator can produce PN11F only, so the Pattern is not selectable.

With the FSYN option, you can select Frame mode. In Frame mode, the Test Generator produces random fill data followed by the specified Frame Sync Word. The length of the fill data plus the sync pattern is the specified Frame Length. In this mode, the Format Synchronizer verifies only the sync pattern portion of the frame, and the Bert Counters (if enabled) include only sync pattern bits in the bit error rate computation.

The other Pattern choices are pseudo-random number (PN) sequences. PN11F is available on all PCI 1601 BSYNs, as well as VME 501-13 and newer. With the BERT option, you can also choose any of PN7F, PN7R, PN9F, PN9R, PN11F, PN11R, PN15F, or PN15R. In PN mode, the Format Synchronizer monitors every bit of the incoming data to establish synchronization. The Bert Counters, if enabled, include every incoming bit in the determination of the bit error rate.

Frame Sync Word (Optional)

Available with the FSYN option. When the Pattern is Frame, enter the sync pattern in hexadecimal. The sync pattern can be up to 24 bits on 501-13 and 601P cards, or 32 bits on 501-21 and newer. Press <enter> or shift the input focus to another control to download the sync pattern.

Frame Length (Optional)

Available with the FSYN option. When the Pattern is Frame, enter the number of bits (32-65536) in the frame.

Frame Sync Mask (Optional)

Available with the FSYN option. When the Pattern is Frame, enter the sync mask in hexadecimal. Setting a bit in the mask enables the corresponding bit in the Frame Sync Word. The maximum mask size is 24 bits on 601P and 501-13 cards, or 32 bits on 501-21 and newer.

To specify a sync pattern shorter than the maximum, turn off the most significant bits in the mask. For example, to specify an 18 bit sync pattern, the mask is 03FFFF.

Fsyn Src (Optional)

Available with the FSYN option. Selects the source to the Format Synchronizer. Decoder selects the clock and data from the BSYN's decoder section. To select Enable DSS, you must choose Decoder as the Fsyn Src. XDAT/XCLK selects external inputs. TestGen selects an internal path from the Test Generator directly to the Format Synchronizer. This is a test selection, which should always cause the Format Synchronizer to report sync.

Enable DSS (Optional)

Available with the FSYN option. Selects Data Source Selection mode, allowing a BSYN to cooperate with a companion BSYN to select between two data sources. Special wiring is required to allow the BSYNs to share Format Synchronizer status.

In DSS mode, the BSYN uses the shared Format Synchronizer status to select its encoder source as either its own decoded data, or data provided at its XCLK/XDAT inputs. Typically, this data is sourced from the companion BSYN. The following table summarizes how BSYN1's DSS will select its encoder source as a function of the shared Format Synchronizer status:

BSYN1 Status	BSYN2 Status	BSYN1's Encoder Source Selection
LOSS	LOSS	No Change
SYNC	LOSS	Decoder Data
LOSS	SYNC	External Data
SYNC	SYNC	No Change

Table 3-8: DSS Mode Source Selection

Auto Polarity (Optional)

Available with the FSYN option. The Format Synchronizer always looks for the sync pattern to have either normal or inverted polarity. When auto-polarity is enabled, the Format Synchronizer automatically inverts the decoder output data (Data output).

Allow Bit Slip (Optional)

Available with the FSYN option. Bit slip is when noisy data produces enough clock jitter to cause a bit period to be added or lost from a frame. Checking this checkbox allows the Format Synchronizer to tolerate a slip of one bit without losing sync. When unchecked, a bit slip results in loss of sync.

Check Errors (Optional)

Available with the FSYN option. Specify the allowed number of Frame Sync Word bit errors in the Format Synchronizers Check state. Choose a value 0-7.

The Format Synchronizer's strategy is to first look for an exact match of the sync pattern. Upon finding one, it then looks for the sync pattern in the next frame. If the number of errors does not exceed the number specified in this control, the Format Synchronizer enters the Lock state.

Note, when synchronizing Test Generator data for a Frame Pattern with Forced Error enabled, allow at least 1 error. Otherwise, the synchronizer will never attain lock.

Lock Errors (Optional)

Available with the FSYN option. Specify the allowed number of Frame Sync Word bit errors in the Format Synchronizers Lock state. Choose a value 0-7. See the Check Errors section for a description of the synchronization strategy.

Note, when synchronizing Test Generator data for a Frame Pattern with Forced Error enabled, allow at least 1 error. Otherwise, the synchronizer will never attain lock.

Bert Period (Optional)

Available with the BERT option. Specify Accumulate to keep a running total of all bit errors, or a period length (1.0En) to display an error rate for each sample of the specified number of bits. The BERT Statistics Display headers automatically change according to the Bert Period mode. The bits included in a test are determined by the Pattern setting. For PN Patterns, all bits are included in the test. When testing Frame data, only bits in the Frame Sync Word are included.

Gen Blanking (Optional)

Available with the BERT option. Allows you to introduce a string of 0 bits into the Test Generator's pattern. See the Encoder Src and Pattern sections for more information about the Test Generator. When the Pattern is Frame, the blanked bits occur immediately following the sync pattern. When the Pattern is a PN sequence, the blanked bits occur each time the generator restarts the sequence. The blanked bits do not introduce errors into the bit error test. If you are using one BSYN to generate the test pattern, and another to count bit errors, you must set their Blanking values the same to avoid blanked bits being counted as errors.

Forced Error (Optional)

Available with the BERT option. Allows you to inject a forced error into the Test Generator's pattern, thus producing a deterministic error rate. See the Encoder Src and Pattern sections for more information about the Test Generator. When the Pattern is Frame, the error bit is the last bit in the sync pattern. When the Pattern is a PN sequence, the error bit occurs once per sequence. Note that when you are using a Forced Error for a Frame Pattern, you should set the allowed Check Errors and Lock Errors to at least one. Otherwise, the synchronizer will never attain lock.

CHAPTER 4

PROGRAMMING BIT SYNCHRONIZERS WITH TDPC

This section describes interfacing to the Acroamatics PCM Bit Synchronizer cards with the `tdpc` compiler. This is an alternative to using the Bit Sync Menu program described previously. With `tdpc`, the BSYN is configured from the host computer by ASCII setup commands that are compiled and transmitted to the card.

TDPC SOFTWARE DESCRIPTION

The `tdpc` setup software for the BSYN cards is written in the C language and is portable to many platforms. The syntax language is compatible with all Acroamatics VME and PCI based telemetry data processors.

At the beginning of a setup, the compiler first reads the current values of all the parameters associated with the specified BSYN and builds a simple table of setup parameters (bit rate, loop width, input source, code type, etc). The compiler then processes the setup text for the BSYN, replacing any old parameter values with the newly assigned ones. At the end of this input, the new table is transmitted to the bit synchronizer - essentially intact and without modification. Any parameters that are not explicitly assigned new values remain unchanged.

The following sections discuss the setup syntax for the BSYN cards.

Multiple Bit Synchronizers

The general form of a BSYN setup program is

```

BITS n
.
.
.
commands
.
.
.
END

```

where n is the unit number of the BSYN you are setting up. If n is omitted, BSYN one is assumed. There are 16 addresses available for BSYNs, which are assigned according to the configuration of the system. `tdpc` can also send the commands to an external bit sync when parameters are added to the configuration file, as described in CHAPTER 2.

Decoder Source Select

Select the decoder input source using the command

```
SRC= $n$  [termination]
```

where n is one of the following values:

<i>n</i>	Description
0	An internal path for a simulator input. Special wiring is required. Check your system documentation to see if you have a simulator, and if it is configured for this option.
1-4	Input connectors IN1-IN4. These are full range common mode or differential (depending upon 2430V configuration) PCM stream input sources. You can also specify the <i>termination</i> as LO or HI impedance.
5	XDAT/XCLK Clock and data are sent from XCLK and XDAT connectors directly to the PCM decoder.
7	Disable all inputs

Table 4-1: Decoder Sources

Source Termination

To select the input source termination, you can use the command

```
TERM z1 z2 z3 z4
```

z1, *z2*, *z3*, and *z4* refer to the termination for inputs 1-4, respectively. Valid *z* values are **LO** or **HI**, which signify 75Ω and 10KΩ terminations, respectively, when the input is configured as single ended. They signify 125Ω and 10KΩ terminations, respectively, when the input is configured as differential. Each of the *z* values must be given.

Decoder Input Codes

Specify the input code type you are going to process by entering the mnemonic as shown below in the Command column.

IRIG Code	Command	Code Definition
NRZ-L	NZL	Non-Return-to-Zero Level
NRZ-M	NZM	Non-Return-to-Zero Mark
NRZ-S	NZS	Non-Return-to-Zero Space
BiP-L	BPL	Bi-phase Level (Split Phase)
BiP-M	BPM	Bi-phase Mark
BiP-S	BPS	Bi-phase Space
DBiP-M	DBI-M	Differential Bi-phase Mark
DBiP-S	DBI-S	Differential Bi-phase Space
DM-M	DMM	Delay Modulation Mark (Miller)
DM-S	DMS	Delay Modulation Space (Miller)
M2-M	M2M	Modified Delay Modulation Mark (Miller)
M2-S	M2S	Modified Delay Modulation Space (Miller)
RZ	RZ	Return-to-Zero
NRZ-L	RNZ-<i>n</i>	Randomized Non-Return-to-Zero Level

Table 4-2: Input Codes

You can apply an IRIG derandomizer to the data after the input code conversion. The run length of the derandomizer is specified on the code line following the input code, as follows:

```
code [n]
```

Specify *code* by using the command from Table 4-2. Run length values for *n* are **9**, **11**, **15**, **17**, or **23**. You need to specify the run length only if you have a randomized code. If you do not specify a derandomizer length, the derandomizer is disabled. The **RNZ-n** command is applicable only for randomized NRZ-L data.

Derandomizer Pattern Direction

Set the direction of the PN pattern applied by the derandomizer using one of the following commands:

FOR Derandomize forward PN patterns
REV Derandomize reverse PN patterns

Use this command along with the input code command (Decoder Input Codes) to decode randomized data. The input code command selects the PCM code and run length, and this command set the the direction of the PN pattern. For example, to decode BiP-L randomized with a PN17R pattern, use the commands

```
BPL 17
REV
```

Bit Rate

Set the bit rate with the command

```
BR=rate
```

You can idle the BSYN by setting the *rate* to 0. Otherwise, valid rates for the VME 501-13 and older cards are in the range 8 bps-20 Mbps for NRZ codes, or 8 bps-10 Mbps for all others. Valid rates for the PCI 1601 and 472 Mezzanine, and 501-22 and newer cards are in the range of 8bps to 32Mbps for NRZ codes, or 8bps to 16Mbps for all other codes, where bps means bits-per-second, and Mbps is million-bits-per-second.

The following are all valid commands for setting a bit rate of 12.34 Mbps.

```
BR=1.234E7
BR=12340000
BR=12340K
BR=12.34M
```

A BSYN will remain in the idle state until a non-zero bit rate is entered and an input source is selected. At that time the BSYN will enter the search state, as indicated by the red status LED on the front panel. Entering a rate of zero will return a BSYN to the idle state, turning off the BSYN status LEDs.

Loop Width

Loop width controls the BSYN PLL's capture range and tracking rate relative to an inputs signal's frequency perturbations. In general, use a smaller loop width for noisy, frequency stable signals, and a larger loop width for signals that may have doppler effects or be subject to tape speed variations.

Set the loop width with the command

```
LW=n.n%
```

The loop width can be set from 0.1% to 3.2% with a resolution of 0.1%, making 32 possible settings.

Loop Tracking

Loop tracking sets the maximum allowable PLL frequency deviation from the programmed bit rate. The larger the numeric value of the loop tracking parameter, the larger the range - except in the case of a 0.0% setting, which disables loop tracking altogether and allows the loop to track over its maximum range.

The command

TRK=*n*.*n*%

sets the loop tracking. The PLL is momentarily reset when the recovered clock rate drifts beyond the $\pm n.n\%$ value. The BSYN provides 100 settings from 0.0% to 9.9%.

Filter Selection

The following filtering functions are available:

- NLF** Selects the narrow bandwidth for the low-pass filter
- WLF** Selects the wide bandwidth for the low-pass filter
- EHF** Enables the high-pass filter
- DHF** Disables the high-pass filter
- OFD** Enables over-filtered data recovery

Generally speaking, the low-pass filter removes noise and perturbations above the BSYN's frequency setting, and the high-pass filter removes signal content below the frequency setting. Using the filters does not necessarily result in better data output, and you should experiment with the filters on noisy signals or tapes. Try the **OFD** command when your data has been severely over-filtered. This command modifies the AGC routine to compensate for the varying amplitude levels of overfiltered signals. Also, the detection circuitry monitors the data peaks rather than the zero crossings on bit rates above 100kbps. This allows you to recover extremely over-filtered data.

Viterbi Input Decoding (Optional)

The BSYN, equipped with any of the above options, decodes data that has been encoded with a K=7, rate $\frac{1}{2}$ convolutional, forward error correcting device. Rate $\frac{1}{2}$ convolutional encoding applies two separate polynomials to seven consecutive bits of data, then forwards the output as two symbols, each symbol being the result of one of the polynomials. The symbol rate is therefore twice the input data rate. The symbols may be transmitted serially using time division multiplexing techniques, or in parallel, using two links (such as a QPSK modulator). Using a history of previous symbols and a maximum-likelihood decoding algorithm, the decoder recombines and processes the symbols to reproduce the original data.

The Viterbi decoder is enabled by the following command line:

VIT [*type*] [*decision*] [*code*] [*modulus*] [*descram*] [**OQ**] [**REV**]

The input type can be serial, with the two symbols alternating in time, or parallel. Decoding parallel inputs with the symbols simultaneously processed requires two BSYNs. One BSYN, designated the slave, produces a soft bit decision and sends it to the other BSYN, designated the master. The Viterbi decoder on the master BSYN takes the soft bit decisions for the two symbols and processes them to reproduce the original data. If *type* is not specified, serial is assumed. *type* is selected by:

- SER** serial
- MAS** master
- SLA** slave

You can set the decoder to accept a hard or soft decision about a given bit. In a hard bit decision, the decoder is simply told that the value of the symbol is 0 or 1. In a soft bit decision, the decoder is given an 8-level value that expresses not only the binary value of a bit, but also a level of confidence with respect to that value. Because the decoder receives more information in a soft bit decision, you get better decoding performance. If decision type is not specified, soft bit decision is assumed. Specify *decision* by

HBD hard bit decision
SBD soft bit decision

The input code can be normal (NRZ-L) or differential (NRZ-M). If it is not specified, normal is assumed. Specify *code* as:

NOR normal
DIF differential

In order to increase the number of binary transitions in a convolutionally encoded data stream, the data may be enhanced with a randomizer or a scrambling algorithm. The BSYN derandomizes the data when you specify a derandomizer modulus. Specify *modulus* as one of **9**, **11**, **15**, **17**, or **23**. If *modulus* is not specified, the derandomizer is disabled. Alternatively, the BSYN supports three scrambling algorithms commonly used with convolutionally encoded data. These are the CCITT V.35 algorithm, the INTELSAT algorithm, and G2 inversion - which simply inverts the G2 symbol generated by the convolutional encoder. You specify *descram* by:

ITT CCITT V.35
INT Intelstat
G2 Invert G2

The BSYN cannot simultaneously derandomize and descramble. If you specify both *modulus* and *descram*, the BSYN will only descramble.

The BSYN also allows you to control the orientation of the G1 and G2 symbols. Specifying **REV** reverses the orientation of G1 and G2. For serial input, this means that G2 precedes G1 in time. For parallel input, this means that the relationship between the G1, G2 symbols, and the master, slave bit synchronizers is reversed. Further, for parallel input, the two input symbols may be staggered a ½ bit period. This is known as *offset QPSK* and can be decoded by specifying **OQ**.

Decoder Output Clock Phase

The NRZ data at the DATA connector is accompanied by a synchronous clock at the CLOCK connector. The phase relationship between this clock and the output data is selectable with the following command:

CLK *n*

where *n* is **0**, **90**, **180**, or **270**, expressing the phase shift in degrees between the start of the NRZ bit interval and the positive transition of the output clock.

Decoder Data Polarity

The following two polarity commands are available:

NOR selects NORMAL polarity
INV selects INVERTED polarity

Encoder Source

The encoder can use either the clock and data recovered from the bit synchronized PCM signal, an external clock and data source connected via the XCLK and XDAT input pins, or the internal test pattern generator. The default source for the output encoder is the recovered clock and data. You can select the external clock and data to be encoded with the command

XDAT [$\pm n$] [*pol*]

where n is either 1 or 2, indicating that the external clock is the bit rate or twice the bit rate, respectively. The sign, - or +, expresses whether the external clock is to be inverted or non-inverted, respectively. If the rising edges of the clock coincide with the transitions of the data, the sign must be +. If the falling edges of the clock coincide with the transitions of the data, the sign must be -. If you do not give the $\pm n$ parameter, the setting will be + for a non-inverted "times-one" clock.

The BSYN allows you to invert the encoder source. Specify *pol* as **INV** for inverted, or **NOR** for normal polarity. If you do not give the *pol* parameter, normal polarity is assumed.

To explicitly select the bit synchronizer decoded output as the source for the encoder, use the command

IDAT [*pol*]

You can select the Test Generator (TGEN) to the encoder with the command

GDAT [*clk*] [*pol*]

The *clk* parameter specifies the TGEN clock source and must be one of the following strings:

<i>clk</i>	TGEN Clock Source
PLL	Bit Sync phase locked loop clock.
EXT	External clock provided at XCLK connector.
1E7	1×10^7 Hz internal rate generator.
5En	5×10^n Hz internal rate generator. $n = 1-6$.
2.5En	2.5×10^n Hz internal rate generator. $n = 1-6$.
1.25En	1.25×10^n Hz internal rate generator. $n = 1-6$.
1En	1×10^n Hz internal rate generator. $n = 1-6$.
SYNTH=rate	Available with the BERT option on 501-22 card version 3 and up. Synthesizes $0.149014\text{Hz} \leq \text{rate} \leq 40\text{e}6\text{Hz}$ with tuning resolution of better than 0.002%. You can specify <i>rate</i> in several different formats. For example, SYNTH=1000000, SYNTH=1e6, and SYNTH=1m all synthesize 1 MBit. When using engineering units, specify "k" for kilobits and "m" for megabits.

Table 4-3: Test Generator Clock Sources

Randomizer Output

You can randomize the data source you have selected into the PCM encoder. To specify the randomizer run length, use the following command:

RAN n

where n defines the randomizer run length. Valid values are **0** (pass through), **9**, **11**, **15**, **17**, or **23**. The randomizer output is provided at the RNRZ connector unless you are convolutionally encoding in parallel mode. The RNRZ connector then provides one symbol of convolutionally encoded data. Note that the BSYN has only one randomizer, and that you can optionally send the randomized data to the TAPE (see TAPE Output) and CODE (see CODE Output) outputs. Changing the run length with this command will change the run length for all outputs using randomized data.

Randomizer Pattern Direction

Set the direction of the PN pattern applied by the randomizer using one of the following commands:

RFOR Randomizer applies forward PN pattern to the data.
RREV Randomizer applies reverse PN pattern to the data.

Since the BSYN only has one randomizer, changing the pattern direction with this command will affect the data at the RNRZ output as well as the TAPE and CODE outputs if they are being randomized. To produce NRZ-L randomized with a PN23R pattern at the RNRZ output, use the commands

```
RAN 23
RREV
```

TAPE Output

The PCM encoder output is provided as a bipolar analog signal at the Bit Synchronizer's TAPE connector. The output code from the encoder is specified by the command

```
OUT code [n]
```

or the command

```
TAPE code [n]
```

Select *code* from the IRIG Code list in Table 4-1.

You can select randomized data to the encoder by specifying the n argument. Specify n as **RAN** to select randomized data to the encoder, but leave the randomizer's run length unchanged. Specify n as a run length **9**, **11**, **15**, **17**, or **23** to select the randomizer output to the encoder, and set the randomizer's run length. Since the BSYN only has one randomizer, changing the run length with this command will also affect the data at the RNRZ output as well as the CODE output if it is being randomized. If you don't specify the n argument, the encoder data will not be randomized, and the randomizer's run length is left unchanged.

For example, to produce NRZ-L randomized with a PN23R pattern at the RNRZ output, and BiP-M randomized with same PN pattern at the TAPE output, use the commands:

```
RAN 23
RREV
TAPE BPM RAN
```

Variable TAPE Output (Optional)

Starting with card version 3 of the 501VA-22, cards equipped with the BERT option can vary the signal amplitude at the TAPE output. Vary the TAPE Output amplitude with the command

```
VTO attenuationDB
```

The *attenuationDB* should be in the range 0-25.5 in steps of 0.1, specifying the amount of attenuation in decibels. The Variable Tape Output command can be used, for example, in BER testing by first setting TAPE attenuation to 0 dB and adjusting your noise level to obtain a starting signal-to-noise ratio. You can then obtain other signal-to-noise ratios by leaving the noise level fixed, and simply adjusting the Variable Tape Output. For example, if you measure your signal-to-noise ratio to be 12dB when *attenuationDB* is set to 0dB, changing the *attenuationDB* to 1dB would give a signal-to-noise ratio of 11dB, *attenuationDB* of 2dB would give a signal-to-noise ratio of 10 dB, 3dB gives 9dB, etc.

CODE Output

The data at the CODE connector is either a TTL version of the data at the TAPE connector, a "pass-through" of the encoder's data source, or convolutionally encoded data. When not convolutional encoding, the CODE connector is set up using one of the following commands

```

CODE TAPE
CODE DATA [n]
CODE NRZ-L [n]
CODE NZL [n]

```

If you specify **TAPE**, the CODE connector will provide a TTL version of the PCM encoded data provided at the TAPE output. **DATA**, **NRZ-L**, and **NZL** are interchangeable. When specified, the CODE connector will provide a TTL version of the encoder source. Further, you can optionally randomize the data by specifying **9**, **11**, **15**, **17**, **23**, or **RAN** for the *n* argument. Specify *n* as **RAN** to select randomized data to the CODE output, but leave the randomizer's run length unchanged. Specify *n* as a run length **9**, **11**, **15**, **17**, or **23**. to select randomized data to the CODE output, and set the randomizer's run length. Since the BSYN has only one randomizer, changing the run length with this command will also affect the data at the RNRZ output (see section Randomizer Output), and possibly the TAPE output (see section TAPE Output). If you don't specify the *n* argument, the CODE data will not be randomized, and the randomizer's run length is left unchanged. By default, the CODE output is a TTL version of the TAPE output.

CKX2 Output

The CKX2 connector provides a programmable clock output. Program it using the command

```
CKX2 multiplier
```

where *multiplier* specifies the multiplier and polarity of the CKX2 output clock relative to the encoder's output data. *multiplier* may take on the values **+2**, **-2**, **+1**, or **-1**. The **+** or **-** specifies that either the rising or falling edges of the clock are coincident with the data bit boundaries. The **2** or **1** specifies the rate multiplier relative to the encoder's input data rate. Use the command described in section Encoder Source to set up the encoder input.

Viterbi Encoding (Optional)

The Viterbi option provides rate ½, k=7 convolutional (Viterbi) encoding. The convolutionally encoded data is provided at the CODE and RNRZ connectors. Use the following two commands to setup the encoder. The first enables and the second disables it.

```

VENC [type] [code] [modulus] [scrambler] [OQ] [REV]
VENC OFF

```

The output type can be serial (with the two symbols alternating in time) or parallel, with the G1 and G2 symbols output simultaneously. Serial data is provided at the CODE connector, while parallel data is provided with the G1 symbol at the CODE connector and the G2 symbol at the

RNRZ connector. If type is not specified, serial is assumed. The commands that define *type* are:

SER for serial output
PAR for parallel output

The output *code* can be normal (NRZ-L) or differential (NRZ-M). If *code* is not specified, normal is assumed. Specify *code* as:

NOR normal
DIF differential

In order to increase the number of transitions in a convolutionally encoded data stream, you can use a randomizer or scrambling algorithm. The BSYN enables randomized data to the Viterbi encoder when you specify the *modulus* argument as **RAN**, or a run length **9**, **11**, **15**, **17**, or **23**. Specifying modulus as **RAN** enables randomized data to the Viterbi encoder without changing the randomizer's run length. Specifying *modulus* as a run length enables randomized data to the Viterbi encoder and sets the randomizer's run length, which will also affect the data at the TAPE output if it is randomized. Alternatively, you can use a scrambler: the CCITT V.35 algorithm, the INTELSAT algorithm, or *G2 inversion*, which simply inverts the G2 symbol generated by the convolutional encoder. To specify a *scrambler*, use one of **ITT**, **INT**, or **G2**. The BSYN cannot both randomize and scramble. If you specify both *modulus* and *scambler*, the randomizer's run length will be set accordingly, but the BSYN will only scramble the convolutionally encoded data.

You can reverse the orientation of the G1 and G2 symbols by specifying **REV**. For serial output, this means that G2 precedes G1 in time. For parallel output, this means that G1 is provided at the RNRZ connector, while G2 is provided at the CODE connector. For parallel output, you can also specify **OQ**, which causes the two symbols to be staggered by a half-bit period. This is known as *offset QPSK*.

Format Generator and Synchronizer (Optional)

You can use the BSYN for generating and verifying data across a link. To generate a source data pattern, the BSYN has a programmable Test Generator (TGEN). You can select it as the encoder source using the **G DAT** command (see the section Encoder Source). Use the format synchronizer (FSYN) to verify the pattern (see the section Format Synchronizer and Data Source Selector (Optional)), and the bit error rate tester (BERT) to count errors and assess link quality (see the section Bit Error Rate Test (Optional)). The TGEN is standard on all VME 501VA-13 and PCI 1601 BSYNs, while the FSYN and BERT are available as options. To work together, the TGEN, FSYN, and BERT share setup that you specify with one of the following commands:

```
FMT PNxy
FMT FRAME LEN=dec SYNC=hex MASK=hex
```

The first form of the command selects PN mode. In this mode the TGEN generates the PN pattern, the FSYN monitors every bit of the incoming data to establish sync, and the BERT includes every bit in its determination of the error rate. Specify the PN pattern using the **PNxy** parameter. All VME 501VA-13 and PCI 1601 BSYNs support **PN11F**. BSYNs with the BERT option support **PN7F**, **PN7R**, **PN9F**, **PN9R**, **PN11F**, **PN11R**, **PN15F**, and **PN15R**.

The second form of the command selects Frame mode. In this mode, the TGEN generates a frame of random fill data followed by the specified sync pattern. The FSYN verifies that sync pattern in each incoming frame of data, while the BERT includes only sync pattern bits in its computation of the bit error rate. Specify the number of bits in the frame with the **LEN=dec** parameter, where *dec* is a decimal number from 32-65536. You specify the sync pattern and mask using the **SYNC=hex** and **MASK=hex** parameters, where the hex values are 24 bit hexadecimal numbers. Setting a bit in the mask enables the corresponding bit of the sync pattern.

To specify a sync pattern of less than 24 bits, turn off the most significant bits of the mask. For example, for an 18 bit sync pattern, set the *hex* value of the mask to 03FFFF.

Programmable Test Generator (Optional)

The Test Generator (TGEN) generates a test pattern that you can select as the source to the encoder (see **GDAT** in the Encoder Source section), and thereby generate data to an external link. Set the format of the TGEN data with the **FMT** command (see the section Format Generator and Synchronizer (Optional)). On BSYNs with the BERT option you can modify the generated pattern using the following command:

```
GEN [ferr] [blanks]
```

The *ferr* parameter allows you to inject a forced error into the pattern, producing a deterministic error rate. Specify *ferr* as follows:

FERR Inject a forced error in test pattern.
ERROFF Disable forced error in test pattern.

In Frame mode, the error bit is the last bit in the sync pattern. In PN mode, the error bit occurs once per sequence of the PN pattern. If not specified, forced error is disabled.

Specify the *blanks* parameter to introduce a string of 0 bits into the test pattern. In Frame mode, the blanked bits occur immediately following each sync pattern. In PN mode, the blanked bits occur each time the generator restarts the PN sequence. The blanked bits will not introduce errors into a bit error test if performed on a BSYN whose GEN is configured with the same number of blanks. The *blanks* value may be one of **64**, **128**, or **256** bits, or **BLOFF** to disable. If not specified, blanking is disabled.

Format Synchronizer and Data Source Selector (Optional)

A BSYN with the FSYN option can verify patterns in incoming data to produce synchronization status, and determine the data's polarity. You can use the synchronization status as a realtime indicator of data quality, and/or use it in the Data Source Selector (DSS) mode in conjunction with another BSYN to automatically select between two data streams. If you have the BERT option, the FSYN will work in conjunction with the BERT to produce bit error rates for PN test patterns by examining every bit, or frame data by examining only sync pattern bits. For information about switching between PN and Frame mode, see the section Format Generator and Synchronizer (Optional).

Setup the FSYN with the commands

```
FSYN [src] [autopol] [slip] [CHECK=x] [LOCK=y] [dss]  

FSYN OFF
```

The *src* argument specifies the FSYN's source, and must one of

DCDR Internal path from Decoder
XDAT XCLK/XDAT inputs
TGEN Internal path from Test Generator

The internal path from the Test Generator is provided as a self-test for the BSYN card. If *src* is not specified, the default is decoder.

The FSYN always looks for the sync pattern to have either normal or inverted polarity. The FSYN can automatically invert the decoded output data when it detects an inverted sync pattern. Specify the *autopol* parameter as

AUTO Enable automatic polarity inversion
NOAUTO Disable automatic polarity inversion

If not specified, auto-polarity defaults to disabled.

Noisy data produces clock jitter that can cause bits to be added or lost from the frame. This is called bit slip. The FSYN has the ability to tolerate a slip of one bit without losing sync. Specify *slip* as

SLIP Allow single bit slip
NOSLIP Disallow all bit slips

If the *slip* argument is not specified, bit slips will force a loss of synchronization status.

Specify the allowed number of sync pattern bit errors using the **CHECK=*x*** and **LOCK=*y*** arguments, where *x* and *y* are numbers in the range 0-7. The FSYN's synchronization strategy is to first look for an exact match of the sync pattern. Upon finding one, the FSYN then looks for the sync pattern in the next frame. If it finds a sync pattern with less than or equal to *x* errors, it enters the synchronized state. If not, it again searches for an exact match of the sync pattern. Once synchronized, the FSYN continues verifying sync patterns until it detects one with more than *y* errors. The FSYN then restarts synchronization by again searching for an exact sync pattern match. If you don't specify the **CHECK=*x*** and **LOCK=*y*** arguments, they default to 1.

Data Source Selection (DSS) Mode allows the BSYN to automatically select between two data sources. DSS mode is supported on the VME 501VA-13 with the FSYN option. In addition, special wiring is required to allow the BSYN to share its status with another BSYN. In DSS Mode, the BSYN will use the shared synchronization status to select its encoder source as either its own decoded data, or data provided at its XCLK/XDAT inputs. Typically, the latter will be sourced from the companion BSYN. The following table summarizes how BSYN1's DSS will select its encoder source as a function of the shared sync status:

BSYN1 Status	BSYN2 Status	BSYN1's Encoder Source Selection
LOSS	LOSS	No Change
SYNC	LOSS	Decoder Data
LOSS	SYNC	External Data
SYNC	SYNC	No Change

Table 4-4: Data Source Selection

Specify the *dss* argument as

DSS Enable DSS Mode (The FSYN source must be decoder.)
NODSS Disable DSS Mode

If not specified, DSS mode defaults to disabled.

Bit Error Rate Test (Optional)

A BSYN with the BERT option can run bit error rate tests on PN patterns. When the BSYN also has the FSYN option, it can also run bit error tests on arbitrary frame data by including only the sync pattern bits in the bit error rate computation. For more information about selecting between PN and Frame mode, see the section Format Generator and Synchronizer (Optional).

Setting up a bit error rate test includes:

1. Using the **FMT** command to select a PN Pattern or Frame parameters (Format Generator and Synchronizer (Optional) section).
2. Using the **GDAT** command to select the Test Generator to the encoder (Encoder Source section). This is not necessary if using an external test pattern generator.

3. Using the **FSYN** command to setup the synchronizer (Format Synchronizer and Data Source Selector (Optional) section). This command is available only when you have the **FSYN** option.
4. Using the **BERT** command to setup the BERT counters (this section).
5. Monitoring and restarting the test as necessary (see the section BERT Statistics Display (Optional) of CHAPTER 3).

The syntax for configuring the BERT is

```
BERT [period]  
BERT OFF
```

The *period* parameter determines whether the BERT runs periodic tests, or continuously checks bits to accumulates the total number of errors. If you selected a PN pattern with the **FMT** command, all bits are included in the test. If you specified Frame mode, then only bits in the sync word are included.

In a periodic test, the BERT checks the specified number of bits and reports the number of errors. The results of the finished period are available until the next period completes, at which time the results are replaced. In an accumulation test, the BERT reports the total number of bit errors that have occurred since the test was started. To set the test type, specify *period* as

```
ACC Accumulation Test  
1En Period Test of  $10^n$  bits. n is in range 3-9.
```

If *period* is not specified, **ACC** is assumed. If you want to disable the BERT, use the **BERT OFF** syntax in your program.

Default Values

To revert to default values for all parameters, use the following command:

```
INIT
```

The parameter default values are listed below.

Source Select	0
Source Termination	LO for all inputs
Input Code	NRZ-L
Derandomizer	OFF
Derand Direction	FOR (forward)
Bit Rate	0
Loop Width	0.3%
Loop Tracking	0.0% (disabled)
Hi Pass Filter	DHF (disabled)
Low Pass Filter	WLF (wide)
Decoder Clock Phase	0 (degrees)
Decoder Data Polarity	NOR (normal)
Encoder Source	IDAT (decoder data)
Randomizer	0 (pass through)
Rand Direction	RFOR (forward)
TAPE Output	NRZ-L
CODE Output	TAPE (encoder output)
CKX2 Output	+2 (0° at $2 \times$ bit rate)
Convolutional Encoding	OFF
TGEN/FSYN Format	PN11F
FSYN	OFF

BERT

OFF

Typical Setup

An example of a typical BSYN setup is shown below.

BITS 1		BEGIN BIT SYNC #1 SETUP
BR=1.2E7		SET BIT RATE TO 12MHz
BPL		SET INPUT CODE TO BIPHASE-L
SRC=1		SELECT INPUT SOURCE 1
LW=1.5%		SET LOOP WIDTH TO 1.5%
NOR		SELECT NORMAL POLARITY
FOR		SELECT FORWARD TAPE DIRECTION
NLF		SELECT LOW PASS FILTER
TAPE DMM		TAPE OUT SET FOR DELAY MILLER MARK
END		END OF SETUP

CHAPTER 5 MONITORING BSYN STATUS

GENERAL

After setting up your Bit Syncs, you can monitor their status using the Bit Sync Status Display. The status display shows one line for each available bit sync. The following example shows a system that has BSYN1-BSYN3, and BSYN5-BSYN8. BSYN4 is not installed, so the status display does not show it.

The screenshot shows a window titled "BitsStat" with a menu bar containing "File" and "Help". The main content is a table with the following data:

UNIT	STAT	AMP	OFFSET	LOOP	FSYN	I/O
BSYN1	IDLE	+00.0V	+00.0V	+00.0%	OFF	ONLINE
BSYN2	IDLE	+00.0V	+00.0V	+00.0%	OFF	ONLINE
BSYN3	IDLE	+00.0V	+00.0V	+00.0%	OFF	ONLINE
BSYN5	IDLE	+00.0V	+00.0V	+00.0%	OFF	ONLINE
BSYN6	IDLE	+00.0V	+00.0V	+00.0%	OFF	ONLINE
BSYN7	IDLE	+00.0V	+00.0V	+00.0%	OFF	ONLINE
BSYN8	IDLE	+00.0V	+00.0V	+00.0%	OFF	ONLINE

UNIT Column

This column displays the unit's name, BSYN#.

STAT Column

This column displays the BSYN's lock status:

IDLE	The BSYN's rate is set to 0Hz, or else the input is disabled (SRC=7 in tdp).
LOSS	The amplitude of the input signal is too small for synchronization to occur (i.e. below 0.1V peak amplitude).
SEARCH	The BSYN is attempting to synchronize with the input signal.
LOCK	The BSYN card is "locked" in synchronization with the input data.
ERROR	The status display encountered an error while trying to communicate with the bit sync card.

Table 5-1: Bit Sync Status Values

AMP Column

This is the input signal's average peak voltage.

OFFSET Column

This is the input signal's average baseline offset voltage.

LOOP Column

This is the input signal's loop stress; its deviation from the programmed bit rate.

FSYN Column

For BSYNs equipped with the FSYN option, this column displays the format synchronizer's status. When the FSYN option is absent, the status reads "OFF", and is grayed-out. When the FSYN option is present, this status is one of the following values:

OFF	FSYN disabled.
LOSS	FSYN not synchronized.
SYN	FSYN is synchronized and data polarity is correct. Auto-polarity is disabled
*SYN	FSYN is synchronized but a bit slip has occurred.
INV	FSYN is synchronized but data is inverted. Auto-polarity is disabled.
*INV	FSYN is synchronized and data is inverted, but a bit slip has occurred. Auto-polarity is disabled.
+SYN	FSYN is synchronized and data polarity is correct. Auto-polarity is enabled.
-SYN	FSYN is synchronized but data is inverted. Auto-polarity is enabled and has corrected the BSYN output data polarity.

Table 5-2: Format Synchronizer Status Values

I/O Column

This describes status of the Status Menu's input/output connection to the BSYN. When "ONLINE", the menu is able to communicate with the BSYN. "OFFLINE" means that the menu cannot communicate with BSYN. This might happen, for example, if the BSYN is in a remote 2430 chassis connected by Ethernet, and the 2430 chassis is powered down. After correcting a communication problem, press the "OFFLINE" button to reconnect the menu to the BSYN.